

High-performance multiprocessor IP for Web-connected digital home SoCs

Baseline Specifications*

Process	MIPS32® 1074Kc™ Core Available in "Kc" (integer) and "Kf" (with floating point)
Frequency ^{1,2}	Fully synthesizable, process independent
Dual-core example implementation:	
Performance	@ 1.25 GHz > 6,300 Total Coremark > 5,000 Total DMIPS
Power (core+L1 caches)	< 1W dynamic power
Area ¹	4.1 mm ²

¹ Optimized for speed, worst case slow/slow corner with production margins, no OD, primarily SVt. Other specs for area/power/process optimized implementations available upon request.

Achieved using commercially-available, non-custom, standard cells from TSMC and memories from Dolphin Technology

² Configuration: dual core, each core with 64 dual entry JTLB and 32KB instruction and data L1 caches, plus coherence management unit (GIC, CPC, IOCU, etc.)

Note: Frequency, power consumption, and size depend upon configuration options, synthesis, silicon vendor, process, and cell libraries.

Key Applications

Web-connected Digital Home

- Digital televisions
- Set-top boxes
- Blu-ray Players

Home/SOHO (Small Office/Home Office)/

Wireless Networking

- Highly-integrated gateway products including support of broadband modem, router, WiFi, VoIP, NAS, and other functions

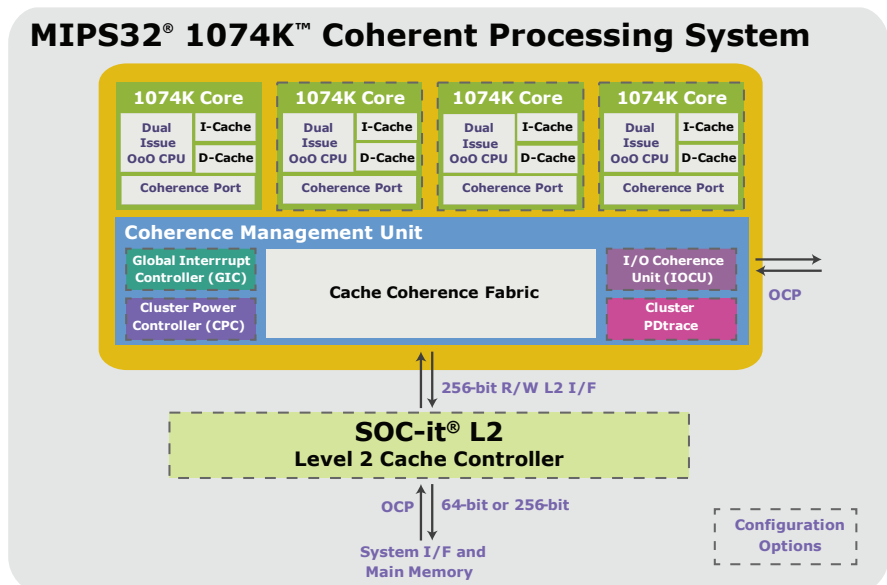
High-End Portable Media Devices/Tablets

- Leveraging the Android™ operating system on the MIPS® architecture

MIPS32® 1074K™

The MIPS32® 1074K™ Coherent Processing System (CPS) is the latest coherent multiprocessor IP offering from MIPS Technologies. The 1074K CPS sets a new standard of performance within MIPS' portfolio of licensable processor core IP, delivering over 15,000 CoreMark and up to 12,000 DMIPS in 40nm technology at 1.5 GHz (worst case slow corner conditions with production margins). The 1074K CPS is available as fully-synthesizable multicore IP that achieves high frequencies using commercially-available, non-custom, standard cells and memories. The 1074K CPS enables easy implementation of very high-performance multicore systems, maximum flexibility in configuration for specific features, and the ability to migrate your design across foundries, process nodes, and geometries.

The 1074K CPS is based on the combination of two high-performance technologies—coherent multiprocessing, and the superscalar, Out-of-Order (OoO) MIPS32 74K™ processor core as the base CPU. The 74K core is a multi-issue, 15-stage OoO architecture already in production with numerous customers for digital televisions, set-top boxes and a variety of home networking applications. The 74K core is broadly used in internet-connected digital home products. To further optimize the core for this growing trend, MIPS Technologies recently enhanced the 74K core to deliver as much as 30% additional performance on JavaScript and Web applications. With the 74K core at its heart, the 1074K CPS is an ideal high-performance platform for today's SoC designs, with headroom for tomorrow's designs as well.



1074K Core Family Highlights

- Foundry process independent, fully-synthesizable, multiprocessor IP supporting very high frequency implementations with commercial, non-custom standard cells and memories
- Cache coherent multiprocessing system supporting configurations with up to 4 cores
- Uses enhanced version of 15-stage superscalar, OoO 74K series core as base CPU, making it an ideal high-performance multiprocessing platform for Web-connected consumer products and highly-integrated home/residential gateways
 - Provides additional 20-30% per core performance over earlier 74K core on JavaScript and Web-connected applications
- Supported by a broad ecosystem of application software and operating systems

Features

A complete system for coherent multiprocessing, including:

- 1 to 4 1074K “base” cores
 - 1074K base core = 74K superscalar, out-of-order high-performance processor with 15-stage pipeline, and cache coherence structures added for interface to Coherence Management unit
- Coherence Management (CM) unit – high throughput coherence fabric supporting 256-bit wide buses internally on key datapaths, as well as external read and write data interfaces to L2 cash and through to rest of system logic in SoC implementation
- I/O Coherence Unit (IOCU) – hardware acceleration for I/O coherence, offloading software implementation on CPUs
- Cluster Power Controller (CPC) – multicore power gating, clock gating, and reset management
- Global Interrupt Controller (GIC) – system and inter-processor interrupt controller
- EJTAG/PDtrace™ block for advanced debug/trace of complete coherent system

Floating Point Unit (FPU)

- MIPS 32® 1074Kf™ core version has IEEE 754-compliant FPU per core, compliant to MIPS® 64-bit FPU architecture
- Supports single- and double-precision data types
- Separate in-order, dual-issue pipeline decoupled from integer pipeline in each core

Coherency Management (CM) Unit

- Manages coherency using the MESI protocol
- Maximized throughput for multicore cluster supported by:
 - 256-bit wide read and write buses (4x bus width between each core and CM) on key internal datapaths
 - 256-bit wide read and write interfaces from CM to L2 cache and through to system interconnect
 - L1 cache-to-cache transfers, speculative reads to external memory, and globalized cache operations
- Global Configuration Registers (GCRs) for configuring/controlling CM scheme

Cluster Power Controller (CPC)

- Provides highly scalable performance/power management via shutdown and bring up of one or more cores in the coherent processing system via clock or voltage island control
- Works in conjunction with each core implemented in a separate power domain

I/O Coherence Unit (IOCU)

- Bridges non-coherent I/O peripheral transfer and makes transactions coherent
- Supports per-transaction attributes for snooping L1 caches, L1+L2 caches, or non-coherent transactions, plus I/O prioritization

Global Interrupt Controller (GIC)

- Supports system-level interrupts; inter-processor interrupts
- Routes interrupts to a particular core or VPE
- Configurable # of system interrupts (up to 256)

Development Tools

- MIPS® Navigator ICS – Integrated Development Environment (IDE), software toolkit, cycle accurate and instruction accurate simulator models, EJTAG and PDtrace probes
- CodeSourcery - SG++ toolchains for MIPS

The performance
of a custom
implementation...
without the
customization

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