

Ideal performance
and power footprint
for mainstream digital
home and portable
media applications

Baseline Specifications*

Product	MIPS32® 24KE™
Process	65 GP TSMC
Frequency^{1,2} (worst case)	900 MHz
Performance	2.31 Coremark/ MHz
	1.51 DMIPS/MHz
Power (mW/MHz) (core+L1 caches)	0.28 mW/MHz
Area¹	1.25 mm ²

¹ Configuration: 32K/32K I/D L1 caches, 32 dual entry JTLB

² Optimized for speed (area and power-optimized specs available upon request)

Achieved using off-the-shelf standard cells from TSMC and memories from Dolphin; quoted speeds include signal integrity analysis, 10% OCV and 50ps PLL jitter margin, worst case slow corner conditions (unless specified).

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries

MIPS32® 24K/24KE™

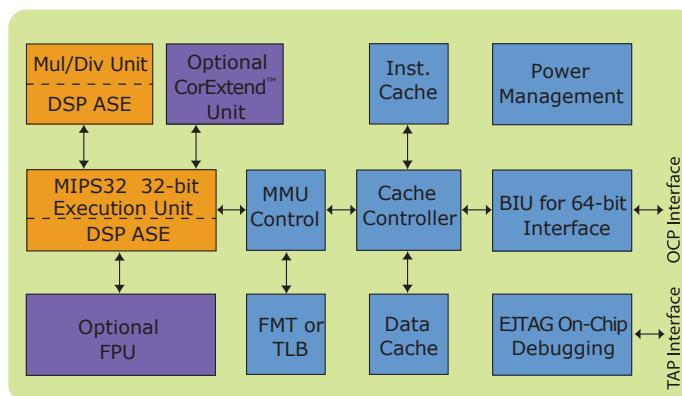
The MIPS32® 24K™ family of cores is a mainstay in the MIPS32-compliant licensable IP cores from MIPS. Supported by licenses to nearly 70 customers and a broad ecosystem, the 24K series provides an extremely competitive balance on excellent performance in an optimal power and area footprint. The 24K family leverages an 8-stage pipeline and high performance microarchitecture, with extensions in the family to tune the processor to your application requirements. Versions within the family include support for hardware accelerated floating point, CorExtend functionality to enable the implementation of User Defined Instructions (UDIs), and DSP acceleration via implementation of the DSP ASE in the 24KE™ series. These instructions improve signal processing performance up to 200 percent over a range of embedded applications when compared to RISC implementations without the DSP ASE.

The 24K series can hit 900 MHz in 65nm, and nearly 1.5 GHz in 40nm process technologies, delivering the robust performance necessary for STB, DTV, BluRay disc, and other digital home applications as web connected operating systems such as Android and functions such as Browsers, Widgets and Flash migrate into these products. The 24K family of cores is supported by a complete suite of software development tools and broad third party ecosystem.

MIPS32 24KE Family Highlights

With an 8-stage pipeline, clock frequencies of 900 MHz in 65nm and scaling to much higher in 40nm, the 24K family of cores enable SoC designers to solve demanding performance requirements, but do so with a very small footprint, efficient, cost effective processor core.

- “f” versions of 24K family cores provide accelerated floating point performance via an IEEE std 754 compliant hardware FPU. Use of the FPU has shown speed-ups of 3x or more in a variety of web-connected benchmarks for javascript performance and web page rendering tasks.
- The DSP ASE implementation in the 24KE series enables increased signal processing performance and functional integration for voice, audio and video applications, simplifying development and reducing overall SoC die area, cost, and power consumption.
- The CorExtend™ feature in this family allows users to supercharge application performance by defining and adding their own instructions.



• **24Kc™ Core:** This base core includes a high-performance 32x32 multiply/divide unit and configurable MMU with TLB or fixed mapping.

• **24KEc™ Core:** This core adds the MIPS DSP ASE to the foundation capabilities of the 24K series.

• **24Kf/24KEf™ Cores:** Include a hardware floating point unit that is fully compliant with IEEE 754.

• **24K/24KE™ Pro Cores:** Pro series cores feature the CorExtend™ capability for user defined instructions

Features

MIPS32 Release 2 Architecture

- 8-stage pipeline
- 32-bit address
- Vectored interrupts and support for external interrupt controller
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)

Floating Point Unit (FPU)

- Floating point version of core available
- IEEE std 754 compliant, supporting single and double precision calculations
- Contains 32 64-bit registers for more operations with less load/store overhead

MIPS32 DSP Architecture (24KE series)

- 4 64-bit accumulators
- 2 control registers
- 64-bit data paths to caches and external interface
- Vectored interrupts and support for external interrupt controller
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)

DSP ASE Instructions

- 8-,16-and 32-bit SIMD instructions
- Saturating and fractional math
- Popular DSP operations, such as MAC, dot-product, absolute and complex-multiply
- Key features such as variable bit insert/extract and virtual circular buffers, complex multiply

DSP ASE Library

- A robust set of key DSP functions, including DCT, FFT, and FIR filters

MIPS16e™ Code Compression

- Reduces memory requirements by as much as 40 percent
- 16-bit encodings of 32-bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines

Programmable Cache Size

- Individually configurable instruction and data caches, sizes of 0KB,16KB, 32KB and 64KB
- 4-way set-associative
- Up to four outstanding non-blocking loads
- Write-back and write-through support
- 32-byte cache line size

Scratch Pad Data RAM Support

- Independent instruction and cache configuration
- 64-bit OCP interface for external access, DMA
- Can support arrays up to 1 MB
- Interface allows back-stalling the core pipeline

Bus Interface Unit (BIU)

- Implements the Open Core Protocol (OCP 2.X)
- 64-bit read and write data buses to efficiently transfer data between memory and L1 caches
- Supports a variety of core/bus clock ratios to give greater flexibility for system implementations (1, 1.5, 2, 2.5, 3, 3.5, 4 or 5)
- 4-entry write buffer

Integer Multiply/Divide Unit (MDU)

- Fully pipelined single-cycle repeat rate for 32X32 MAC instructions

Power Control

- Minimum frequency: 0 MHz
- Power-down mode (triggered by WAIT instruction)
- Support for software-controlled clock divider
- Support for extensive use of local gated clocks

EJTAG Debug

- Support for single stepping
- Virtual instruction and data address breakpoints
- PC and data tracing with PDtrace™ option

General Purpose Coprocessor (COP2) Interface

- 64-bit interface to a user-defined coprocessor

**900-MHz performance
@ 250mW in 65nm
process technology**

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