

MIPS32® 24KE™

DSP functionality
for enhanced
system-level
performance and
reduced SoC costs

The MIPS32® 24KE™ core family leverages the high performance 24K® microarchitecture while incorporating the MIPS® DSP Application-Specific Extension (ASE). These instructions improve signal processing performance up to 200 percent over a range of embedded applications when compared to RISC implementations without the DSP ASE. The distinguishing feature of the 24KE family is that it provides very efficient DSP capability while significantly reducing overall SoC die area, cost and power consumption.

The 24KE core family is supported by a complete suite of software development tools, the MIPS DSP Library and a third-party DSP applications network. This enables SoC designers to work in a single design environment and decrease system costs by migrating DSP functionality onto a 24KE core.

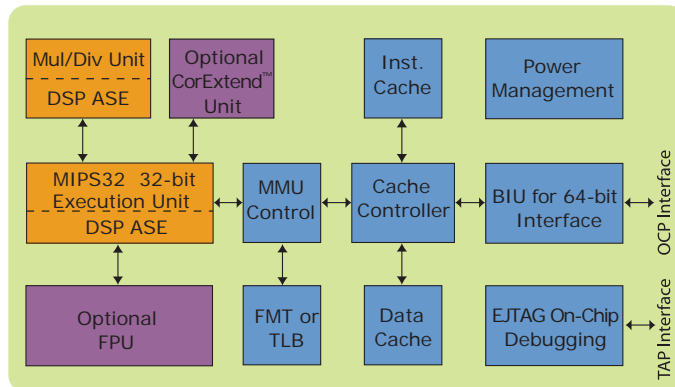
Baseline Specifications

Product	MIPS32® 24KE™
Process	65 GP TSMC
Frequency* (MHz) (worst case)	775 MHz
Performance (DMIPS/MHz)	1.55
Power (mW/MHz @ 1.2V) (core only)	.216
Core area (mm ²) (core only)	0.886 mm

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries.

MIPS32 24KE Family Highlights

- A very efficient DSP ASE implementation allows the 24KE core to act as a DSP-enhanced host core, displacing functionality and dedicated resources from other proprietary processors or DSP cores.
- The combined DSP and host functionality significantly reduces overall SoC die area, cost, and power consumption.
- With up to a 625 MHz host plus DSP performance, the 24KE core enables multimedia and communications applications to be subsumed into a single, simplified design environment.
- Based on the industry-standard 24K microarchitecture, the 24KE family leverages the existing MIPS32 design ecosystem and targets key applications software from voice to video.
- The CorExtend™ capability of the 24KE Pro cores allows users to supercharge application performance by defining and adding their own instructions.



- **24KEc™ Core:** This base core includes a high-performance 32x32 multiply/divide unit and configurable MMU with TLB or fixed mapping.
- **24KE™ Core:** Adds hardware floating point support that is fully compliant with IEEE 754.
- **24KE™ Pro Cores:** 24KEc Pro and 24KEf Pro cores feature the CorExtend™ capability.

Features

MIPS32 DSP Architecture

- 4 64-bit accumulators
- 2 control registers
- 64-bit data paths to caches and external interface
- Vectored interrupts and support for external interrupt controller
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)

Floating Point Unit (FPU)

- Floating point version of core available
- IEEE std 754 compliant, supporting single and double precision calculations
- Contains 32 64-bit registers for more operations with less load/store overhead

DSP ASE Instructions

- 8-, 16- and 32-bit SIMD instructions
- Saturating and fractional math
- Popular DSP operations, such as MAC, dot-product, absolute and complex-multiply
- Key features such as variable bit insert/extract and virtual circular buffers, complex multiply

DSP ASE Library

- A robust set of key DSP functions, including DCT, FFT, and FIR filters

MIPS16e™ Code Compression

- Reduces memory requirements by as much as 40 percent
- 16-bit encodings of 32-bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines

Programmable Cache Size

- Individually configurable instruction and data caches, sizes of 0KB, 16KB, 32KB and 64KB
- 4-way set-associative
- Up to four outstanding non-blocking loads
- Write-back and write-through support
- 32-byte cache line size

Scratch Pad Data RAM Support

- Independent instruction and cache configuration
- 64-bit OCP interface for external access, DMA
- Can support arrays up to 1 MB
- Interface allows back-stalling the core pipeline

Bus Interface Unit (BIU)

- Implements the Open Core Protocol (OCP 2.X)
- 64-bit read and write data buses to efficiently transfer data between memory and L1 caches
- Supports a variety of core/bus clock ratios to give greater flexibility for system implementations (1, 1.5, 2, 2.5, 3, 3.5, 4 or 5)
- 4-entry write buffer

Integer Multiply/Divide Unit (MDU)

- Fully pipelined single-cycle repeat rate for 32X32 MAC instructions

Power Control

- Minimum frequency: 0 MHz
- Power-down mode (triggered by WAIT instruction)
- Support for software-controlled clock divider
- Support for extensive use of local gated clocks

EJTAG Debug

- Support for single stepping
- Virtual instruction and data address breakpoints
- PC and data tracing with PDtrace™ option

General Purpose Coprocessor (COP2) Interface

- 64-bit interface to a user-defined coprocessor

625-MHz performance,
accelerated
time-to-market

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