

600+ MHz
performance,
accelerated
time-to-market

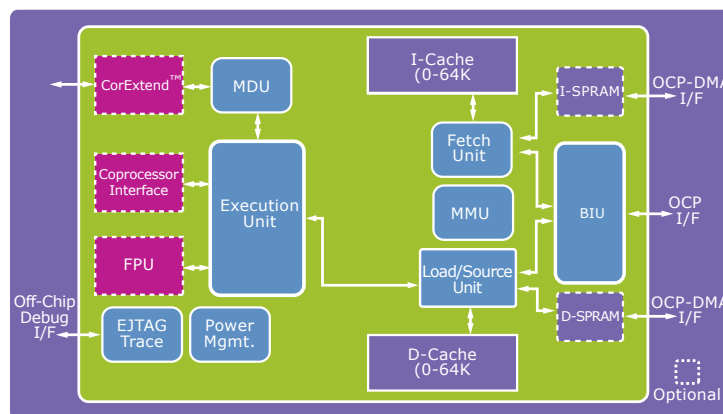
Baseline Specifications*

| | |
|------------------------------------------------------------------------------------------------------|-------------------|
| Product | MIPS32® 24K™ Core |
| Process | 65nm G |
| Frequency* (MHz) (worst case) | 750+ |
| Performance (DMIPS/MHz) | 1.51 |
| Power (mW/MHz) | 0.34 |
| Core Area (mm²) (core only, extracted from fully laid-out GDSII database) | 0.83 |

Note: Frequency and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries

MIPS32® 24K™

Designed to power through graphics, Java and demanding code and with features like an ultrafast multiply/divide unit (MDU), intelligent caches, a high-performance floating-point unit and the CorExtend™ capability—which allows users to accelerate application performance by defining and adding their own instructions—the MIPS32® 24K™ family is the ideal solution for high-performance and low-power applications such as digital and interactive television, set-top boxes, DVD, home networking, GPS, and portable audio and video.



- **24Kc™ Core:** This base core includes a high-performance 32x32 multiply/divide unit and configurable MMU with TLB or fixed mapping
- **24Kf™ Core:** Adds hardware floating point support that is fully compliant with IEEE 754
- **24K Pro Cores:** 24Kc Pro and 24Kf Pro cores feature the CorExtend capability

MIPS32 24K Family Highlights

With an 8-stage pipeline and a maximum clock frequency exceeding 600 MHz in 90nm, the 24K family of cores enable SoC designers to reduce product costs and speed time-to-market by giving them the performance headroom to implement more features now and upgrades in the future with software flexibility rather than rigid, fixed hardware.

Cadence, Synopsys, Magma and other EDA industry leaders help minimize design time and offer a proven path to silicon by co-developing tailored SoC design methodologies. This couples the high-performance, low-power 24K cores with cutting-edge core hardening technologies.

By standardizing the core interface on OCP (www.ocpip.org), the 24K cores accelerate time-to-market by enabling easy reuse of standard SoC IP. Memory controllers, bus interconnects and other standardized peripherals are now easily integrated through common on-chip interfaces.

The highly-scalable 24K microarchitecture implements the industry-standard MIPS32 Release 2 architecture, which includes features such as enhanced bit-field manipulation, reduced interrupt latency and enhanced cache control.

A rich environment of third-party tools and software support the 24K family of cores.

Features

MIPS32 Release 2 Architecture

- 8-stage pipeline
- 32-bit address
- Vectored interrupts and support for external interrupt controller
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)

Floating Point Unit (FPU)

- Floating point version of core available
- IEEE std 754 compliant, supporting single and double precision calculations
- Contains 32 64-bit registers for more operations with less load/store overhead

MIPS16e™ Code Compression

- 16-bit encoding of 32-bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines

Programmable Cache Size

- Individually configurable instruction and data caches, sizes of 0KB, 8KB, 16KB, 32KB, and 64KB
- 4-way set-associative
- Up to eight outstanding load misses
- Write-back and write-through support
- 32-byte cache line size

Scratchpad SPRAM Support

- Independent cache configuration
- 64b OCP 2.1 memory interface
- Can support arrays up to 1MB
- Separate RAMs for instruction and data

Memory Management Unit (MMU)

- 4-entry instruction, 8-entry data micro-TLBs
- Configurable 16/32/64 dual-entry joint TLB with variable page sizes
- Optional fixed mapping translation (FMT) for applications not requiring address mapping or protection

Bus Interface Unit (BIU)

- Implements the Open Core Protocol (OCP) Release 2.1
- 64-bit read and write data buses to efficiently transfer data between memory and L1 caches
- Supports a variety of CPU-to-system bus clock ratios to give greater flexibility for system implementation
- 4-entry write buffer

Integer Multiply/Divide Unit (MDU)

- Fully pipelined single-cycle repeat rate for 32x32 MAC instructions

Power Control

- Minimum frequency: 0 MHz
- Power-down (sleep) mode (triggered by the software WAIT instruction)
- Support for software-controlled clock divider
- Fine-grain clock gating

EJTAG Debug

- Performance counters
- Support for single stepping
- Virtual instruction and data address breakpoints
- PC and data address and value tracing with trace compression

General Purpose Coprocessor (COP2) Interface

- 64-bit interface to a user defined coprocessor

The design solution
for high-performance,
low-power SoCs

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