



MIPS32® 34K®

The MIPS32® 34K® core family is a revolutionary implementation of the MIPS® Multi-threading (MT) Application Specific Extension (ASE) designed to exploit Multi-threading in embedded applications. Processing multiple software threads in parallel, 34K cores take advantage of the effect of memory latency to deliver significant gains in system performance and cost savings, with a minimal increase in die size. The 34K core family gives users the system performance gain of multiprocessing cores in a single core solution.

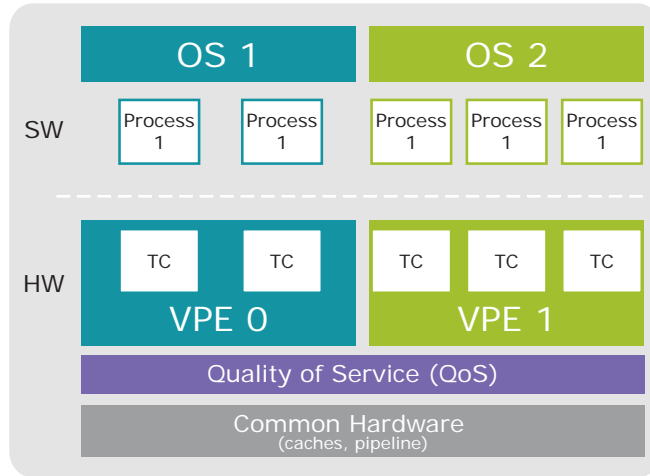
Baseline Specifications

Product	MIPS32® 34Kc® Core
Process	65nm G
Frequency (MHz) (worst case)	704
Power (mW/MHZ) Core only	0.24
Core area (mm²) Core only, extracted from full layout GDSII database	1.02

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries

Configuration: One VPE and two TCs, 32K/32K caches

MIPS32 34K Core—Simplified Overview



TC: Thread Context—represents the user-state of the MIPS32 architecture

VPE: Virtual Processing Element—represents the OS-only visible state of the MIPS32 architecture

MIPS32 34K Family Highlights

Lower System Costs

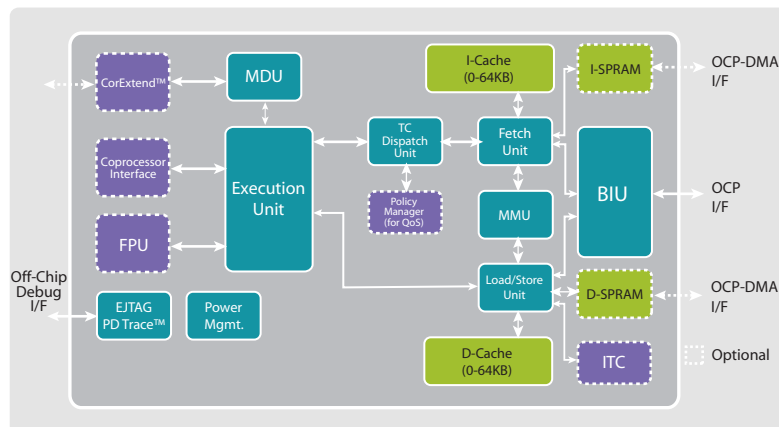
Higher application throughput enables several functions to be consolidated onto a single 34K core while preserving existing investments in software.

Design Flexibility

The 34K core can be configured with a maximum of two VPEs and nine TCs for ultimate design flexibility. Depending on the application, the 34K core can implement symmetric multiprocessing across two VPEs. Alternatively, each VPE can run a separate operating system.

Faster Time-to-Market

A rich environment of third-party tools and software supports the 34K core family.



34Kc™ core: The base core implementing the MIPS® MT and DSP ASEs

34Kf™ core: Adds hardware floating-point support that is fully compliant with the IEEE 754 specification

34K Pro cores: 34Kc Pro and 34Kf Pro cores feature the CorExtend™ capability

Features

MIPS32 Architecture

- 9-stage pipeline
- 32-bit address
- 64-bit data paths to caches and external interface

MIPS MT ASE

- Support for up to 2 VPEs and 9 TCs
- Policy manager for QoS scheduling
- Inter-thread communication memory for efficient message and data transfer between TCs

MIPS DSP ASE

- 3 additional pairs of Hi/Lo accumulator registers
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2×16b or 4×8b simultaneously

Floating Point Unit (FPU)

- Floating point version of core available
- IEEE std 754 compliant, supporting single and double precision calculations
- Contains 32 64-bit registers for more operations with less load/store overhead

Programmable Memory Management Unit (MMU)

- 16/32/64 dual-entry JTLB per VPE
- JTLBs are sharable under software control
- 4-9 entry MT-optimized ITLB; 8-entry DTLB
- Optional simple fixed mapping translation (FMT) mechanism

Programmable L1 Cache Sizes

- Individually configurable instruction and data caches, sizes of 0/8/16/32/64KB
- 4-way set associative
- Up to nine outstanding loads
- Write-back and write-through support
- Cache line locking support

Scratchpad RAM (SPRAM) support

- Separate RAMs for instruction and data
- Two 64-bit OCP interfaces for external DMA

Bus Interface Unit (BIU)

- OCP interface with 32-bit address and 64-bit data
- OCP interface runs at core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4, 5, or 10

Multiply/Divide Unit (MDU)

- 32×32 multiply with a repeat rate of one per clock cycle

Coprocessor 2 Interface

- 64-bit interface to a user-designed coprocessor
- Optional thread support

CorExtend

- Allows user to define and add instructions to the core at build time

Power Control

- Minimum frequency: 0 MHz
- Power-down mode (automatic and program-controlled)
- Software-controlled clock divider
- Extensive use of fine-grained clock gating

EJTAG Debug

- Support for single stepping
- Instruction address and data address/value breakpoints
- TAP controller is chainable for multi-CPU debug
- PC, data address and data value tracing with compression (PDtrace™)

MIPS16e™ Code Compression

- Reduces memory requirements by as much as 40 percent

First synthesizable
multi-threading
solution for
high-performance
applications

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