

First synthesizable
multi-threading
solution for embedded
synthesizable CPUs

Baseline Specifications*

Product	MIPS32® 34Kc™ Core
Process	65nm GP
Frequency^{1,2} (worst case)	850 MHz
Performance	2.92 Coremark/MHz 1.62 DMIPS/MHz
Power (core+L1 caches)	0.3 mW/MHz
Area¹	<1.5 mm ²

¹ Configuration: Two VPEs and two TCs, 32K/32K I/D L1 caches, 32 dual entry JTLB

² Optimized for speed (area and power optimized specs available upon request)

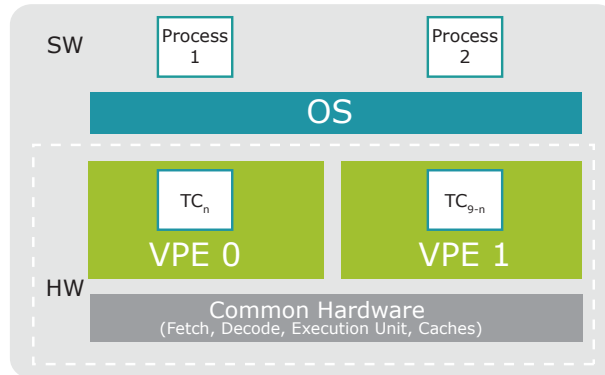
Achieved using off-the-shelf standard cells from TSMC and memories from Dolphin; quoted speeds include signal integrity analysis, 10% OCV and 50ps PLL jitter margin, worst case slow corner conditions (unless specified).

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries

MIPS32® 34K™

The MIPS32® 34K™ core family is the first implementation of the MIPS® Multi-threading (MT) Application Specific Extension (ASE) in a licensable IP core, designed to exploit multi-threading in embedded applications. Processing multiple software threads in parallel, 34K cores take advantage of the effect of memory latency to deliver significant gains in system performance and cost savings, with a minimal increase in die size. The 34K core family gives users the system performance gain of multiprocessing cores in a single core solution.

MIPS32 34K Core—Simplified Overview



Virtual Processing Element

- Looks like complete CPU to SW
- Can run an OS/RTOS
- Build-time option: 1 or 2

MIPS32 34K Core Family Highlights

Leading Performance/Power Efficiency

The 34K core was forged from the 24K series, incorporating the MIPS Multi-threading ASE into an already highly popular microarchitecture. Not surprisingly, the combination of these two technologies provides leading performance power efficiency, delivering 2500 Coremarks at 850 MHz in 65nm, and over 4200 Coremarks at nearly 1.5 GHz in 40nm at ~ 250mW dynamic power in either process.

Design Flexibility

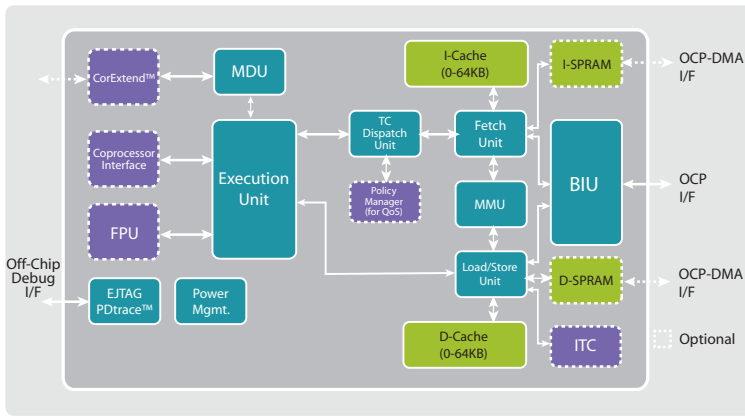
The 34K core can be configured with a maximum of two VPEs and nine TCs for ultimate design flexibility. Higher application throughput enables several functions to be consolidated onto a single 34K core while preserving existing investments in software. Depending on the application, the 34K core can implement symmetric multiprocessing across two VPEs. Alternatively, each VPE can run a separate operating system.

Thread Management Features

The 34K core includes additional features that aide in maximizing the use of hardware threads. A Policy Manager provides prioritization on threads in either round robin or fixed policy mode. The core also supports Inter-Thread Communication (ITC) between TCs via a number of communication methods (mailboxes, FIFO mailboxes, mutexes, semaphores)

Faster Time-to-Market

A rich environment of third-party tools and software supports the 34K core family.



34Kc™ core: The base core implementing the MIPS® MT and DSP ASEs

34Kf™ core: Adds hardware floating-point support that is fully compliant with the IEEE 754 specification

34K Pro Series™ cores: 34Kc Pro™ and 34Kf Pro cores feature the CorExtend™ capability

Features

MIPS32 Architecture

- 9-stage pipeline
- 32-bit address, 64-bit data paths to caches and external interface
- 6 Multiply/Divide Unit (MDU) - 32x32 multiply with repeat rate of one per clock cycle

MIPS MT ASE

- Support for up to 2 VPEs and 9 TCs
- Policy manager for QoS scheduling
- Inter-thread communication memory for efficient message and data transfer between TCs

MIPS DSP ASE

- 3 additional pairs of Hi/Lo accumulator registers
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2x16b or 4x8b simultaneously

Floating Point Unit (FPU)

- 34Kf core version of includes IEEE std 754 compliant FPU, support for single and double precision calculations
- Contains 32 64-bit registers for more operations with less load/store overhead

Programmable Memory Management Unit (MMU)

- 16/32/64 dual-entry JTLB per VPE JTLBs sharable under software control
- 4-9 entry MT-optimized ITLB; 8-entry DTLB
- Optional simple fixed mapping translation (FMT) mechanism

Programmable L1 Cache Sizes

- Individually configurable instruction/data caches, 0-64KB 4-way set associative

Scratchpad RAM (SPRAM) support

- Separate RAMs for instruction and data with 64-bit OCP interfaces for external DMA

Bus Interface Unit (BIU)

- OCP interface with 32-bit address and 64-bit read and write data buses
- OCP interface runs at core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4, 5, or 10

Customizable features: Coprocessor 2 Interface and CorExtend

- 64-bit interface to a user-designed coprocessor or CorExtend allows users to define and add instructions to the core at build time

Power Control

- Minimum frequency: 0 MHz
- Power-down mode (automatic and program-controlled)
- Software-controlled clock divider
- Extensive use of fine-grained clock gating

EJTAG Debug

- Support for single stepping
- Instruction address and data address/value breakpoints
- TAP controller is chainable for multi-CPU debug
- PC, data address and data value tracing with compression (PDtrace™)

The multi-threading
solution for
high-performance
applications

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