High Performance,
Low Power,
Next Generation
32-Bit Cores

Baseline Specifications

Product	MIPS32 4KEc core
Process	130nm
Frequency (MHz) (Worst case)	100 - 252
Max. Performance (DMIPS)	408
Power (mW/MHz)	
Core only	0.15 - 0.37
with 8K/8K caches (Typical)	0.32 - 0.68
Core area (mm^2)	
Core only	0.52 - 1.03
with 8K/8K caches	1.23 - 1.89

Product	MIPS32 4KEc core
Process	90nm
Frequency (MHz) (Worst case)	248 - 424
Max. Performance (DMIPS)	687
Power (mW/MHz)	
Core only	0.15 - 0.26
with 8K/8K caches (Typical)	0.08 - 0.16
Area (mm^2)	
Core only	0.65 - 1.18
with 8K/8K caches	0.33 - 0.69

Note:
Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries. For 130nm, Worst case is slow silicon, 1.08V, 125C; Typical case is typical silicon, 1.2V, 25C. For 90nm, Worst case is slow silicon, 0.9V, 125C, Typical case is typical silicon, 1.0V, 25C.

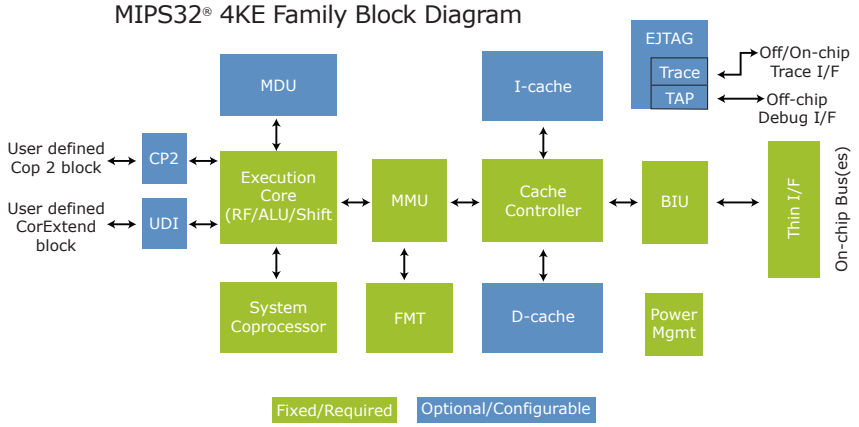
Quoted speeds don't contain OCV, clock jitter and design margin.

MIPS32® 4KE®

The highly configurable MIPS32® 4KE® core family represents the next generation of 32-bit MIPS® cores. With features such as code compression, larger writeback cache memories and extensive clock gating, the 4KE core family gives system-on-chip (SoC) designers flexibility to optimize their applications by maximizing performance or minimizing power consumption.

The 4KE core family sets a new standard for 32-bit synthesizable cores. It offers the highest 32-bit performance available in a synthesizable core with more than 1.5 Dhrystone MIPS/MHz. It also provides configurable features that allow designers to further increase performance while reducing die size and power consumption and, ultimately, total system cost.

MIPS32® 4KE Family Block Diagram



MIPS32 4KE Core Family Highlights

- The 4KE core family includes the following cores:
  - 4KEp® core - basic version with iterative multiply and small fixed mapping translation (FMT) for memory management unit (MMU)
  - 4KEm® core - 4KEp core plus fast Multiply/Divide Unit,
  - 4KEc® core - 4KEm core plus TLB MMU,
  - 4KEPro cores - 4KE cores with CorExtend™ capabilities
- MIPS16e™ code compression allows designers to reduce the memory requirements for their application by as much as 40%.
- Cores can be configured with up to 64KB instruction and 64KB writeback data cache for more flexibility and higher performance.
- The highly configurable and synthesizable core enables flexibility for designers to include only those features necessary for their application.
- Extensive clock gating reduces power consumption without reducing application performance.
- BIST, scan and Enhanced JTAG (EJTAG) debug with trace (PDtrace™) and fast download enable quick and easy debugging.
- The 4KE cores are synthesizable and can be ported to any foundry process.
- All major operating systems and compiler tool chains, and hundreds of third-party development tools support the MIPS® architecture.

Features

MIPS32® enhanced (Release 2) architecture
- 5-stage pipeline
- 1, 2, 4 or 8 sets of 32-bit general purpose registers
- Supervisor mode operation
- Vectored interrupts and support for external interrupt controller
- Atomic interrrupt enable/disable
- Bit field manipulation instructions
- Virtual memory support (small page sizes and hooks for extensive page table manipulation)

MIPS32 privileged resource architecture
- Count/compare registers for real-time interrrupts
- I and D watch registers for SW breakpoints

MIPS16e™ code compression
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
- 16-bit encodings of 32-bit instructions to improve code density

Programmable cache sizes
- Individually configurable instruction and data caches, sizes from 0-64KB
- Direct mapped, 2-, 3- or 4- way set associative
- Loads block only until critical word is available
- Non-blocking prefetches
- Write-back support
- 16-byte cache line size

Scratchpad RAM support
- Can optionally replace 1 way of the I- and/or D-cache with a fast scratchpad RAM
- 20 index address bits allow access of arrays up to 1MB
- Interface allows back-stalling the core

Memory management unit (MMU)
- 32 dual-entry JTLB with variable page size
- Fixed or TLB-based MMU, dependent on family member

Simple bus interface unit (BIU)
- All I/O fully registered
- Separate unidirectional 32-bit address and data buses
- Two 16-byte collapsing write buffers
- Designed to allow easy conversion to other bus protocols

Integer multiply/divide unit (MDU)
- Fast or area-efficient, dependent on family member
- Maximum issue rate of one 32x16 multiply per clock (fast MDU)
- Maximum issue rate of one 32x32 multiply every other clock (fast MDU)

General purpose coprocessor (COP2) interface
- 32-bit interface to an external coprocessor

Power control
- Minimum frequency: 0 MHz
- Power-down mode (triggered by WAIT instruction)
- Support for software-controlled clock divider
- Support for extensive use of local gated clocks

EJTAG debug
- Support for single stepping
- Virtual instruction and data address breakpoints
- PC and data tracing add with trace compression (PDtrace™)
- Cross-CPU breakpoint support

Development tools
- MIPS SDE – GNU based toolchain optimized to support MIPS cores
- MIPSsim™ – bus-functional modeling and instruction-set simulator
- System Navigator™ probe – EJTAG probe
- NavigatorIDE – Eclipse-based graphical integrated development environment

4KE® Cores:
The New Standard in Synthesizable Cores

Worldwide Offices

Headquarters
MIPS Technologies, Inc.
1225 Charleston Road
Mountain View, CA 94043-1353
United States
Phone: 650-567-5000
www.mips.com
info@mips.com

MIPS Technologies (Shanghai) Co., Ltd.
Shanghai, China
Phone: +86 21 6385 8383
Fax: +86 21 5306 0833

MIPS Technologies B.V.
Taipei, Taiwan
Phone: +886 3 6583 561
Fax: +886 3 6583 563

MIPS Technologies B.V.
Tokyo, Japan
Phone: +81 3 5733 9541
Fax: +81 3 5733 9545

MIPS Technologies B.V.
Remscheid, Germany
Phone: +49 2191 900 200
Fax: +49 2191 900 208

MIPS Technologies B.V.
Haifa, Israel
Phone: +972 4 851 5080
Fax: +972 4 851 5090

MIPS Verified™