

Easy-to-use and
cost-efficient family
of cores for SoC
applications

Baseline Specifications

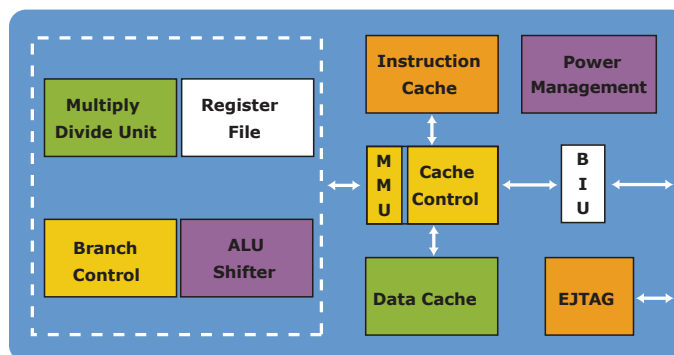
Product	MIPS32 4K core
Process	0.18 μm G
Frequency (MHz) (Worst case)	90–167
Max. Performance (DMIPS)	232
Power (mW/MHz)	1.3–2.2
Core area (mm ²) Core only	1.4–2.5

Notes:

Frequency, power consumption and core size depend upon configuration, synthesis, foundry, process and cell libraries.

MIPS32® 4K™

The MIPS32® 4K™ family of cores is designed for system-on-chip (SoC) applications that require an easy-to-use and cost-efficient embedded processor. These synthesizable and configurable cores have been successfully implemented in hundreds of SoC designs. A rich infrastructure of tools, software and applications make fast time-to-market a reality, while upward compatibility with MIPS64®-based cores ensures a seamless migration path for future system upgrades.



The MIPS32® 4K™ family of cores is designed for semiconductor manufacturers, ASIC developers and system OEMs who want to increase performance, simplify system integration and enjoy scalability across future process technologies in their SoC applications.

MIPS32 4K Core Highlights

- Silicon-proven technology with hundreds of successful implementations reduces time-to-market and increases first-pass success.
- Based on the MIPS32 architecture-enabling cost-effective, leading-edge applications with its high-performance, 32-bit, 5-stage pipeline.
- Synthesizable, configurable and process portable, increases system platform flexibility and longevity.
- Designed for easy SoC integration with a single clock, fully static, flop-based design.
- Fast, single-cycle 32x16 multiplier supports basic DSP functionality.
- Optional EJTAG simplifies debug and shortens time-to-market.
- Upwards compatible with MIPS Technologies 64-bit cores, enabling future system upgrades.
- Supported by hundreds of third-party development tools, software and applications for fast time-to-market and a shortened design cycle.

Features

4K family includes three cores:

- 4Kp™ core — base version with iterative multiply and small FMT MMU
- 4Km™ core — 4Kp core plus fast Multiply/Divide Unit
- 4Kc™ core — 4Km core plus TLB MMU

32-bit MIPS32 architecture

- 32-bit address and datapaths
- 5-stage pipeline
- 32 general-purpose registers

Memory Management Unit

- 16 dual-entry Translation Lookaside Buffer (4Kc)
- Fixed Mapping Translation Unit (4Km, 4Kp)

Configurable 4-way set-associative caches

- 0–16KB instruction cache
- 0–16KB data cache
- 1-, 2-, or 4-way set-associativity
- 16-byte cache line size

Fully static design

- Allows on-the-fly clock changes
- Reduces power consumption
- Minimizes process sensitivity
- Simplifies layout and timing closure

Enhanced JTAG (EJTAG)

- Non-intrusive real-time debugging
- Single stepping
- Instruction and Data breakpoints

Optimized for SoC integration

- Uses off-the-shelf cell libraries and memories
- Instruction and data caches can be configured

Signal interfaces are fully registered for easy implementation

- Non-intrusive, real-time debugging
- Single stepping
- Instruction and Data breakpoints

Simple Bus Interface Unit (BIU)

- All I/Os fully registered
- Separate unidirectional 32-bit address and databases
- Designed to allow easy conversion to other protocols

Power Control

- Minimum frequency 0 MHz
- Software-controlled power-down mode (triggered by WAIT instruction)
- Fine-grain clock gating

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