

First fully-synthesizable
processors to achieve
operating frequencies
greater than 1080 MHz
in a 65nm GP process

Baseline Specifications*

Product	MIPS32® 74Kc™ (standard)
Process	40nm G
Libraries	TSMC 10 track SVt
Frequency^{1,2} (worst case)	>2.5 GHz (typical) 1080 MHz
Performance	2.5 Coremark/MHz 2.0 DMIPS/MHz
Power (core+L1 caches)	0.54mW/MHz
Area¹	1.2 mm ² (core + L1 I/D caches, fully placed, routed)

¹ Both implementations optimized for speed (area and power-optimized specifications available upon request)

² Achieved using free standard cells from TSMC and memories from Dolphin; quoted speeds are at worst case slow/slow corner, with signal integrity and production margins of 10% OCV and 50 ps clock jitter.

Note: Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor and process and cell libraries.

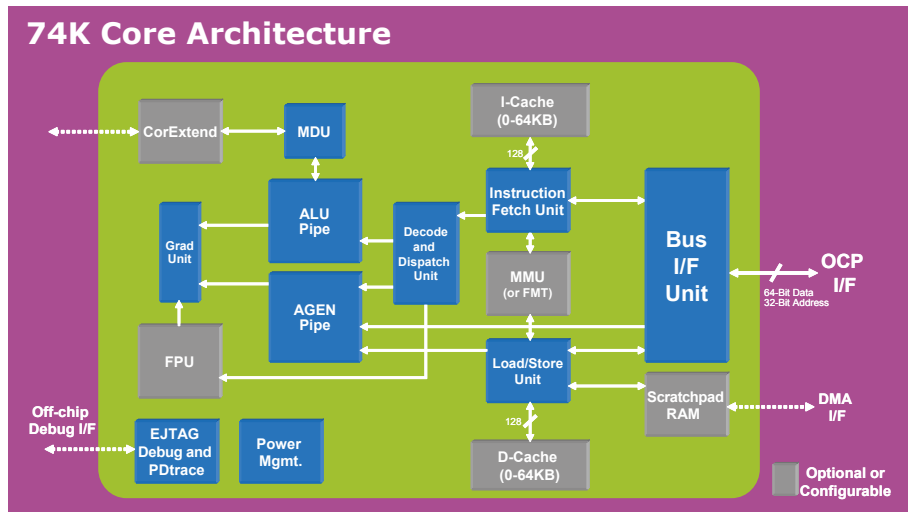
Configuration: 74Kc with 32K/32K caches, 32 entry dual TLB, and no scratchpad

MIPS32® 74K™

The first fully synthesizable IP core to surpass 1 GHz in 65nm process technology just got faster. In 40nm process technology with off the shelf 12 track libraries from TSMC, the MIPS32® 74K™ processor core can achieve frequencies in excess of 2.5 GHz in typical corner and conditions.. The processor family is optimized to deliver exceptional performance as well as the area- and power-efficiencies required for today's complex SoC Designs. This innovative processor technology is interface- and binary-compatible with the industry-standard MIPS32® 24K™, 24KE™ and 34K™ processors, enabling SoC designers to take advantage of their existing software and hardware infrastructure.

The 74K series is uniquely designed to meet the increasingly performance intensive requirements migrating into high-volume applications throughout the digital and connected home. The 74K series has the muscle for the job, whether it's running a web browser and/or Flash player on an Android-based DTV, set-top box, or HD-DVD, or running router, WiFi, VoIP and NAS software stacks in an integrated home gateway with high speed broadband connectivity.

The 74K core family is designed to work with generic standard cells, memories and EDA design flows without the need for premium physical IP or costly structured logic and custom design flows. Out-of-order dispatch provides superior performance on existing binary code, without the need to recompile.

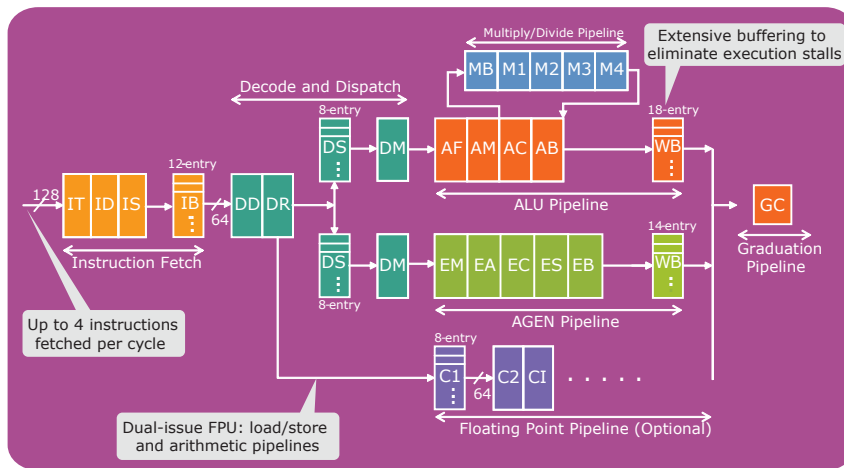


Designed for Maximum Configurability, Area-Efficiency and Processing Power

74K Core Family Highlights

- A 15-stage asymmetric dual-issue pipeline, out-of-order (OoO) instruction dispatch/completion and fully synthesizable design gives SoC developers full porting flexibility across different processes and accelerating time-to-market
- 74Kf version provides accelerated floating point performance via an IEEE std 754 compliant hardware FPU. Use of the FPU has shown speed-ups of 3x or more in a variety of web-connected benchmarks for javascript performance and web page rendering tasks.
- Standard OCP bus interface provides backward-compatibility with existing 24K, 24KE and 34K cores
- A rich ecosystem of third-party software and debug tools coupled with software and tools support from MIPS Technologies

74K Processor Core Pipeline



Features

Architecture

- Superscalar asymmetric dual-issue pipeline with OoO dispatch and completion supported with completion buffering and renaming scheme
- MIPS32 Release 2 ISA compliance with large 32 logical register set, extended for OoO operation through completion buffer and renaming scheme
- Support for optional multiple copies of the General Purpose Registers (GPRs) via shadow register set(s) for high priority interrupts and exception handling
- Support for Revision 2 of the MIPS32 DSP ASE
- 128-bit access to the I-cache and 64- or 128-bit wide access to the D-cache
- Up to 4 instructions fetched per cycle
- Combined majority branch predictor using three 256-entry BHT; 8-entry return prediction stack
- CorExtend™ user-defined instruction set extensions
- Multiply/divide unit to support maximum issue rate of one 32/32 multiply per clock
- Low power support via fine grain, block level, and top level clock gating
- MIPS16e™ code compression
- EJTAG debug 3.2 interface and PDtrace™ program and data trace

Floating Point Unit (FPU)

- 74Kf FPU compliant with IEEE 754 and MIPS® 64-bit FPU architecture
- Supports single- and double-precision data types
- Separate in-order, dual-issue pipeline decoupled from integer pipeline

Bus Interface Unit

- OCP version 2.1 interface with 32-bit address and 64-bit read/write data busses
- Interface supports core/bus clock ratios of 1, 1.5, 2, 2.5, 3, 3.5, 4, 5, or 10

Programmable MMU

- 16/32/48/64 dual-entry, dual-ported TLB shared by Instruction and Data MMU
- 4-entry ITLB (4KB, 1MB page size)
- Optional simple Fixed Mapping Translation (FMT) mechanism

Programmable Cache Sizes

- Configurable I-Cache (0-64KB) and D-Cache (0-64KB) sizes
- 4-way set-associative caches with write-back and write-through support
- 32-byte cache line size
- Data scratchpad RAM support (4KB-1MB)

Development Tools

- MIPS Navigator™ ICS - IDE, SW toolkit, MIPSsim™, EJTAG and PDtrace probes
- CodeSourcery - SG++ toolchains for MIPS

Industry-leading
performance
with advanced
microarchitecture
and enhanced
DSP capabilities

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