

High-performance processor core optimized for MCU and real-time embedded applications with microMIPS™

Baseline Specifications

Product	MIPS32 M14K core	
Process	TSMC 130G SVt	
Performance	1.5 DMIPS/MHz	
	Speed Opt	Area Opt
Frequency (MHz)	190	100
Core area (mm ²)	0.68	0.35
Power (mW/MHz)	0.22	0.12

Product	MIPS32 M14K core	
Process	TSMC 90G Svt	
Performance	1.5 DMIPS/MHz	
	Speed Opt	Area Opt
Frequency (MHz)	329	200
Core area (mm ²)	0.51	0.21
Power (mW/MHz)	0.12	0.06

Note:
Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries

Quoted speeds do not contain OCV, design margin and clock jitter

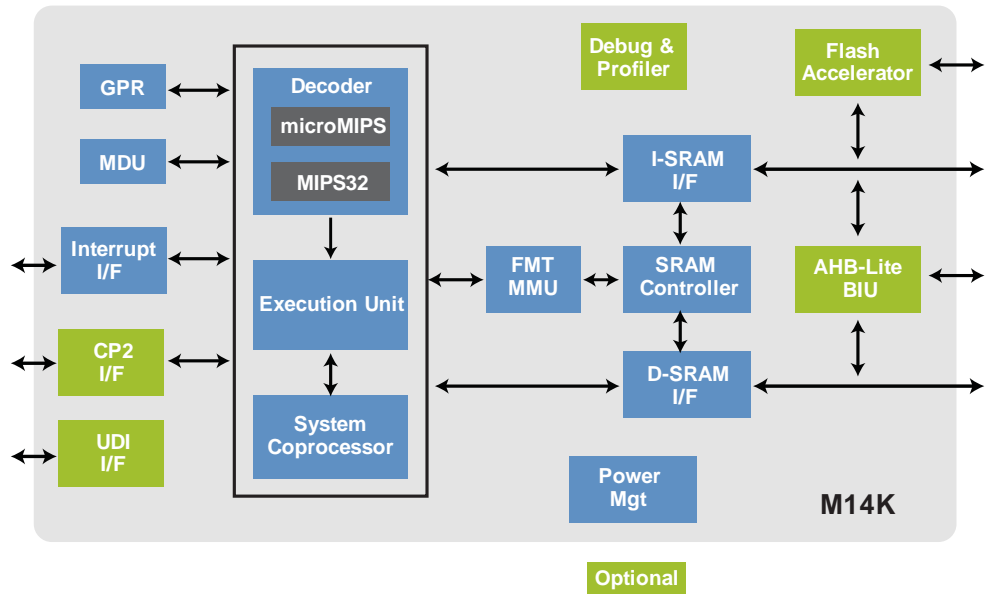
Key Applications:

Microcontroller & Embedded Control

- Standard microcontroller
- Industrial control
- Smart meter
- Automotive body and chassis
- Home appliances
- Wired connectivity
- Wireless connectivity
- Power supply, battery management
- Touch screen controller
- LCD controller/driver
- Printers
- Storage

MIPS32® M14K™

The MIPS32® M14K™ core offers a high-performance, low-power and compact processor core architecture that provides an optimized, low-cost solution for a wide range of microcontroller (MCU) and real-time embedded applications. The M14K core executes the microMIPS™ instruction set architecture (ISA), achieving a performance efficiency of 1.5DMIPS/MHz with an advanced level of code compression. The M14K core includes enhanced features such as low latency interrupt handling, accelerated flash memory access and comprehensive debug capabilities that address the requirements of advanced MCU and embedded system design.



MIPS32 M14K Core Highlights

- Best in class performance at 1.5 DMIPS/MHz
- Highly optimized processing engine scalable across the frequency range
- Designed on the 4K® micro-architecture, proven in millions of SoCs
- microMIPS ISA achieves 35% code size reduction and 98% performance of MIPS32
- Supports MIPS32 Release 2 architecture
- Includes legacy MIPS32 instruction decoder
- 10 cycle interrupt latency; automated interrupt prologue, interrupt epilogue and interrupt chaining
- Pre-fetch logic reduces access times to slower, flash-type memory
- Comprehensive debug and trace features decrease development time and enhance design verification
- Easy connection to a wide range of application-specific peripherals through AMBA AHB-Lite Bus Interface Unit
- Highly configurable and extendable, offering a wide range of implementation options to minimize cost and maximize reusability
- Optimized architecture with the smallest area and lowest power consumption relative to competitive solutions

Features

MIPS32 Release 2 Architecture

- 5 stage pipeline
- Up to 16 sets (configurable) of 32x32-bit general purpose registers
- Vectored interrupts, and support for an external interrupt controller
- Fixed Mapping Translation (FMT) memory management unit
- MIPS32-compatible instruction set

microMIPS™ Instruction Set Architecture

- Enhanced code compression scheme (maximum performance), implementing a variable length encoding of 16- and 32-bit instructions
- Supports all existing MIPS32 instructions, except branch likely instructions
- New 16- and 32-bit instructions added to reduce overall code size
- MIPS32 assembly level and ABI compatible
- Integrated support for Privileged Resource Architecture
- Includes all MIPS ASE instructions, and supports UDI space

MCU-ASE

- Extends the number of interrupt pins from 6 to 8 in Vectored Interrupt mode
- Supports up to 255 interrupts in External Interrupt Controller mode
- Includes hardware features to reduce interrupt latency: interrupt vector pre-fetching, automatic save COPO registers and use of Shadow registers
- Includes new IRET instruction that automates interrupt return handling operations
- Provides support for interrupt chaining (optional)
- Includes 2 new atomic memory to memory instructions, ASET (atomic bit set) and ACLR (atomic bit clear)

SRAM Style Interface

- 32-bit address and data, input byte enables simple connection to narrower memory buses
- Separate or unified instruction and data memory interfaces
- I-SRAM and D-SRAM parity support 1-bit per byte (optional)
- Single or multi-cycle latencies
- Deterministic timing

Optimized Interface for Flash Memory

- Instruction pre-fetch buffer
- Configurable memory address range and bit width

Multiply & Divide Unit

- Configurable, performance or area optimized
- Single cycle 32x16 multiply, 2 cycle 32x32 multiply
- Divide operation latency between 11 and 34 clock cycles

AHB-Lite Bus Interface Unit (optional)

EJTAG Debug & Trace

- Enhanced iFlowtrace™ support with PC and/or data trace with compression, including trace of function call returns, hardware execution and data triggers
- Simple instruction & data breakpoint detection support: 2I/1D, 4I/2D, 6I/2D, 8I/4D
- Complex breakpoints, instruction & data, with conditional filtering supported
- Support for 2 performance counters (PC) with multiple event type options
- PC and data address sampling: zero overhead, qualified read/write
- Fast debug channel provides a low overhead, high bandwidth bi-directional data transfer capability between the target and debug host/probe
- Support for single stepping
- EJTAG interface operates through a TAP control port

Power Management

- Extensive use of fine grain clock gating
- Power down mode, initiated by Wait instruction or under register control
- Reduce operating frequency through a software controlled clock divider

Extension Interfaces

- COP2 32-bit general purpose coprocessor interface
- CorExtend™ capability to develop user defined instructions

Features microMIPS –
minimum code size,
maximum performance

Worldwide Offices

Headquarters
MIPS Technologies, Inc.
955 East Arques Avenue
Sunnyvale, CA 94085
United States
Phone: 408-530-5000
Fax: 408-530-5150
www.mips.com
info@mips.com

MIPS Technologies (Shanghai) Co., Ltd.
Shanghai, China
Phone: +86 21 6385 8383
Fax: +86 21 5306 0833

MIPS Technologies B.V.
Hsinchu, Taiwan
Phone: +886 3 6583 561
Fax: +886 3 6583 563

MIPS Technologies B.V.
Tokyo, Japan
Phone: +81 3 5733 9541
Fax: +81 3 5733 9545

MIPS Technologies B.V.
Remscheid, Germany
Phone: +49 2191 900 200
Fax: +49 2191 900 208

MIPS Technologies B.V.
Haifa, Israel
Phone: +972 4 851 5080
Fax: +972 4 851 5090



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