

High-performance,  
microMIPS™  
enhanced processor  
core with integrated  
cache controller

## Baseline Specifications

<b>Product</b>	MIPS32 M14Kc core	
<b>Process</b>	TSMC 90G SVt	
<b>Performance</b>	1.5 DMIPS/MHz	
	<b>Speed Opt</b>	<b>Area Opt</b>
<b>Frequency (MHz)</b>	340	200
<b>Core area (mm<sup>2</sup>)</b>	0.82	0.37
<b>Power (mW/MHz)</b>	0.15	0.08

### Note:

Frequency, power consumption and size depend upon configuration options, synthesis, silicon vendor, process and cell libraries.

Quoted speeds do not contain OCV, design margin and clock jitter

## Key Applications:

### Home entertainment:

Digital TV (DTV)  
Set-top box (STB)

### Home networking:

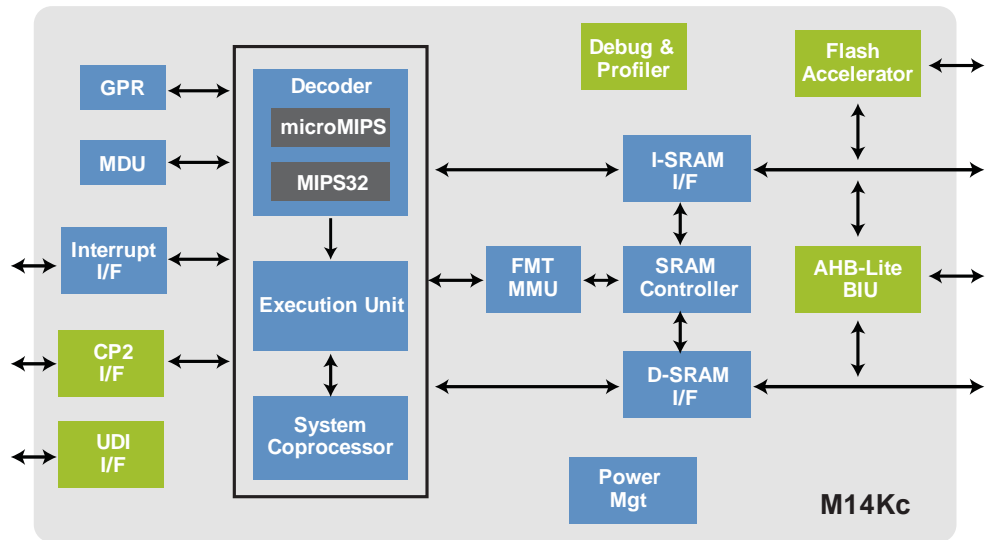
Residential gateway (RG)  
WiFi router  
Voice over internet protocol (VoIP)  
Network attached storage (NAS)

### Personal entertainment:

Digital camera (DSC)  
Digital video recorder (DVC)  
Personal media player (PMP)  
Personal navigator (PND/GPS)  
Digital photo frame (DPF)

# MIPS32® M14Kc™

The MIPS32® M14Kc™ processor core offers a high-performance, low-power and compact architecture with advanced features optimized for media-rich, real-time embedded applications such as those in home entertainment, personal entertainment, and home networking. The M14Kc core executes the new microMIPS™ instruction set architecture (ISA), achieving a performance efficiency of 1.5DMIPS/MHz with a high level of code compression. The M14Kc is based on the popular 4KEc™ micro-architecture, enhanced with additional features such as reduced interrupt latency, enhanced MMU, parity support, comprehensive debug capabilities and AHB-Lite bus interface unit.



Optional

## MIPS32 M14Kc Core Highlights

- Best in class 1.5 DMIPS/MHz performance 5-stage pipeline core
- Designed on the 4K® micro-architecture, proven in millions of SoCs
- Supports MIPS32 Release 2 architecture and MIPS32 instruction decoder
- Integrated cache controller; separate I- and D-cache
- microMIPS ISA achieves 35% code size reduction and 98% performance of MIPS32
- Memory Management Unit (MMU), Translation Lookaside Buffer (TLB)
- 10 cycle interrupt latency; automated interrupt prologue, epilogue and interrupt chaining
- AMBA AHB-Lite Bus Interface Unit
- Comprehensive debug and trace features, enhancing design verification and reducing development time
- Scratchpad RAM (SPRAM) support (optional)
- Parity support for I- and D-cache and SPRAM (optional)
- Highly configurable and extendable, offering a wide range of implementation options to minimize cost and maximize reusability
- Power management
- On-chip co-processor (CP2) and CorExtend™/user defined instruction (UDI) interfaces
- CodeSourcery SG++ software toolchain support
- Development support; System Navigator™ probe, MIPS Navigator™ Integrated Component Suite (ICS), SEAD-3 development board, cycle and instruction accurate simulators

## Features

### MIPS32 Release 2 Architecture

- 5 stage pipeline, 4K micro-architecture
- Up to 16 sets (configurable) of 32 x 32-bit general purpose registers
- Vectored interrupts with support for an external interrupt controller
- Support for shadow register sets (configurable)
- MIPS32-compatible Instruction Set

### microMIPS™ Instruction Set Architecture

- Enhanced code compression scheme (maximum performance), implementing a variable length encoding of 16- and 32-bit instructions
- Supports all existing MIPS32 instructions, except branch likely instructions
- New 16- and 32-bit instructions added to reduce overall code size
- MIPS32 assembly level and ABI compatible
- Integrated support for Privileged Resource Architecture
- Includes all MIPS ASE instructions, and supports UDI space

### MCU-ASE (Application Specific Extension)

- Extends the number of interrupt pins from 6 to 8 in Vectored Interrupt mode
- Supports up to 255 interrupts in External Interrupt Controller mode
- Includes hardware features to reduce interrupt latency: interrupt vector pre-fetching, automatic save COPO registers and use of shadow registers
- Includes new IRET instruction that automates interrupt return handling operations
- Provides support for interrupt chaining (optional)
- Includes 2 new atomic memory to memory instructions, ASET (atomic bit set) and ACLR (atomic bit clear)

### Programmable Cache Controller

- Individually configurable I- and D-caches, sizes range from 0 to 64KB
- Direct mapped 2-, 3- or 4-way set associative with write-back and write-through support
- 16-byte cache line size

### Memory Management Unit (MMU)

- 4 entry instruction and data TLB (ITLB/DTLB) with variable page sizes
- 16- or 32 dual entry joint TLB (JTLB) with variable page sizes
- Fixed or TLB-based MMU
- Security attribute: read-inhibit and execute-inhibit

### Multiply & Divide Unit

- Configurable performance or area optimized
- Single cycle 32x16 multiply, 2 cycle 32x32 multiply
- Divide operation latency between 11 and 34 clock cycles

### AHB-Lite™ Bus Interface Unit

- Supports single bus master mode
- 2 unidirectional 32-bit data buses for read and write operations
- Burst read/write and single read/write modes supported

### Parity Support (optional)

- Parity detection for I- and D-cache, I- and D-SPRAM

### EJTAG Debug & Trace

- Enhanced iFlowtrace™ support with PC and/or data trace with compression, including trace of function call returns, hardware execution and data triggers
- Simple instruction & data breakpoint detection support: 2I/1D, 4I/2D, 6I/2D, 8I/4D
- Complex breakpoints, instruction & data, with conditional filtering supported
- Support for 2 Performance Counters (PC) with multiple event type options
- PC and data address sampling: zero overhead, qualified read/write
- Fast debug channel provides low overhead, high bandwidth bi-directional data transfer capability between target and debug host/probe

### Power Management

- Extensive use of fine grain clock gating
- Power down mode, initiated by Wait instruction or under register control
- Cache memory power saving mode

Delivers a feature-rich,  
optimized solution  
for embedded  
applications, with  
maximum code density

## Worldwide Offices

Headquarters  
MIPS Technologies, Inc.  
955 East Arques Avenue  
Sunnyvale, CA 94085  
United States  
Phone: 408-530-5000  
Fax: 408-530-5150  
www.mips.com  
info@mips.com

MIPS Technologies (Shanghai) Co., Ltd.  
Shanghai, China  
Phone: +86 21 6385 8383  
Fax: +86 21 5306 0833

MIPS Technologies B.V.  
Hsinchu, Taiwan  
Phone: +886 3 6583 561  
Fax: +886 3 6583 563

MIPS Technologies B.V.  
Tokyo, Japan  
Phone: +81 3 5733 9541  
Fax: +81 3 5733 9545

MIPS Technologies B.V.  
Remscheid, Germany  
Phone: +49 2191 900 200  
Fax: +49 2191 900 208

MIPS Technologies B.V.  
Haifa, Israel  
Phone: +972 4 851 5080  
Fax: +972 4 851 5090



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