

FPGAView™ Software for Debugging Xilinx FPGA Devices with Tektronix Logic Analyzers and Mixed Signal Scopes

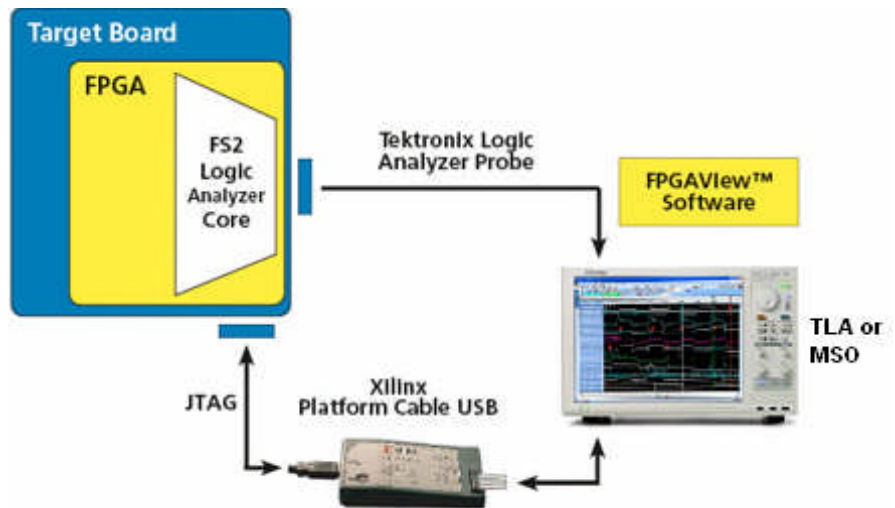
FPGAView™ software from First Silicon Solutions (FS2) works with the Tektronix® TLA series of logic analyzers and MSO4000 series of Mixed Signal Oscilloscopes to enable real-time debugging of Xilinx FPGAs. Using FPGAView software, you can quickly and easily trace signals inside the Xilinx® FPGA design and select which group of internal signals to probe without having to recompile the design. FPGAView software simplifies logic analyzer use by automatically updating TLA and MSO channel names when a new bank of signals is selected for tracing.

System Overview

The diagram (above right) shows the complete interconnection of target, JTAG cable, Tektronix TLA or MSO, and FPGAView software. The logic analyzer probes plug into the target board for accessing the on-chip FPGA signals that are brought out of the device and wired to probe connectors, or to a connectorless probe site. The TLA, a PC in itself, runs FPGAView and hosts the Platform Cable USB connected between the PC USB port and Xilinx JTAG target connector. For any of the MSO4000 series oscilloscopes, FPGAView runs on a PC and communicates to the MSO over Ethernet or USB. In both cases, the FPGAView software controls which on-chip signal bank is routed to the external probe connectors, updates bank signal names associated with each logic analyzer channel, and reads or writes the General Purpose (GP) input/output signals.

FS2 Logic Analyzer Core (LA Core)

FPGAView includes a configurable logic analyzer core (LA Core), an IP block that connects internal signals to device pins, provides a multiplexer to select one of multiple banks of signals, provides timing or state



measurement modes, and supplies general purpose inputs and outputs with values scanned in and out over the JTAG connection.

The LA Core provides the user the choice of internally connecting to either USER1 or USER2 JTAG port for internal communications. For Virtex4 and 5 devices, all four USER ports are available to choose from.

Hardware Cable Control

The Platform Cable USB is the Xilinx target cable used by FPGAView software to control the Logic Analyzer Core. This is the same JTAG hardware port controlled by the Platform Cable USB and driven by Xilinx tools to handle functions like programming the FPGA device, loading Flash, or controlling on-chip microprocessors.

OCI Generator (OCIGen™)

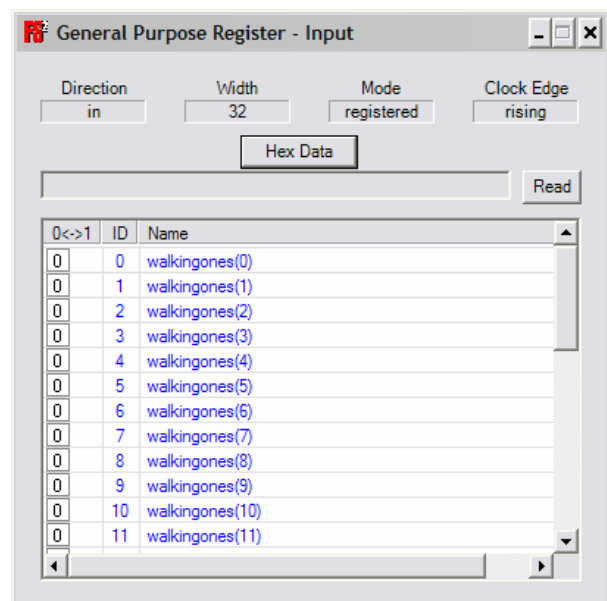
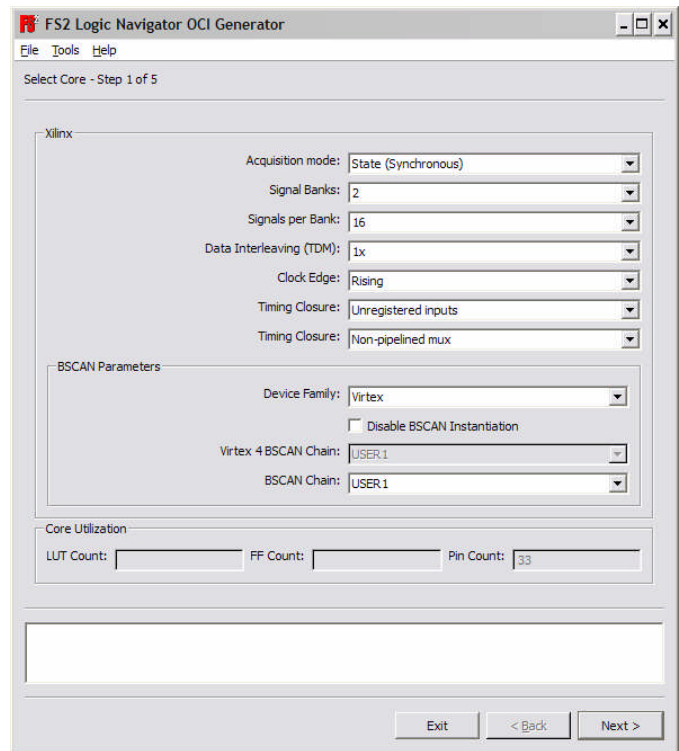
Included in the FPGAView package is the OCIGen program – On-Chip Instrumentation Generator. This program sets up the parameters that configure the LA Core, connects the user signals that are to be probed to the core, and installs them into the user's root HDL file. After connecting the desired internal signals, the user runs the

instrumented design through the standard synthesis, place & route, and .bit file generation stages.

OCIGen is a wizard-centric GUI program that makes it easy to select various core parameters such as signals per bank, number of banks, acquisition mode, and clock edge. It then directs the user to select HDL files (Verilog or VHDL) and scans the files to extract available signal names. In the next step, the user selects the desired signals to probe and which LA Core bank to connect them to. Clicking on “Connect” wires them up. The last step is to click on “Generate” which inserts the core into the top-level HDL file and adds the signal assignment statements that wire up the clock and signals. It handles “percolating” signals from lower levels in a hierarchical design to the top level where the LA Core has been inserted.

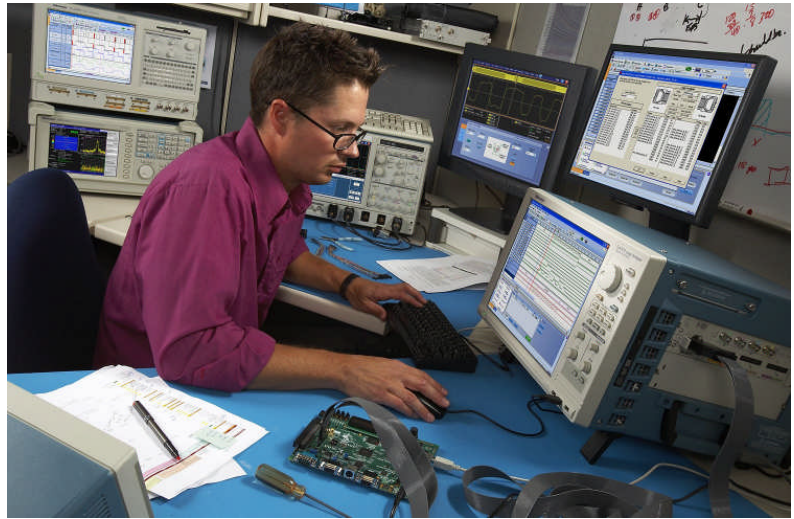
General Purpose Input/Outputs

The LA Core IP block includes support for general purpose inputs and outputs. These GP inputs and outputs can be specified in groups of 8 channels up to 64 channels. Once defined and synthesized into the core, FPGAView can view the GP inputs by a click of a button, and any value can be set into the GP outputs with the same GUI. GP inputs can provide visibility into internal states. GP outputs can be used to set signals inside the device for debug control, mode selection, or simple pattern generation. Examples could be controlling a gated clock, setting the clock speed, or single-cycling the clock.



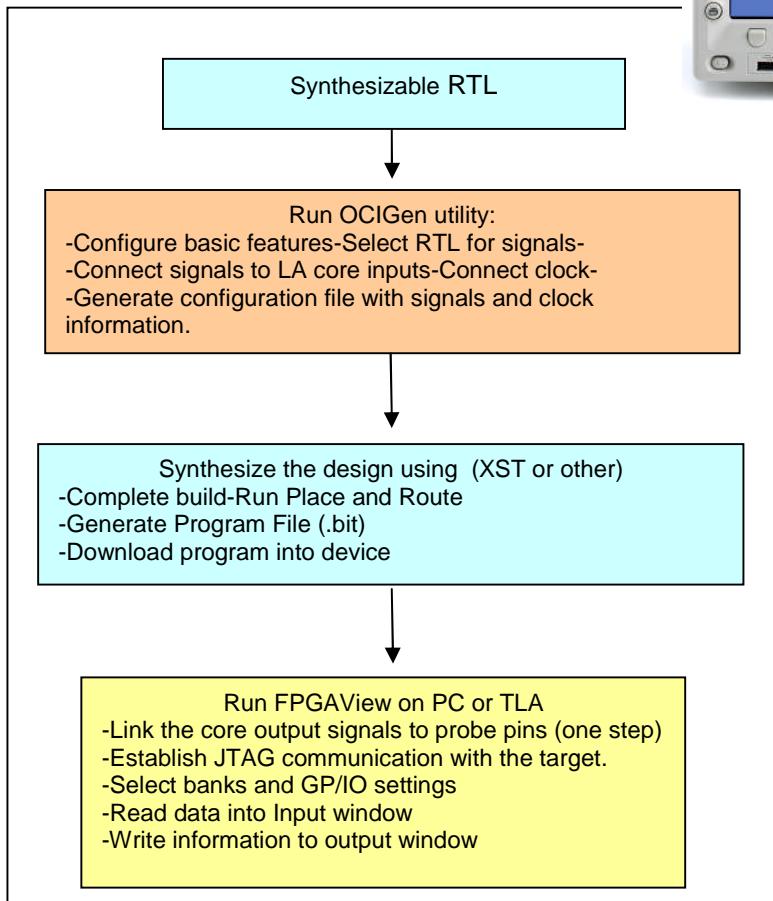
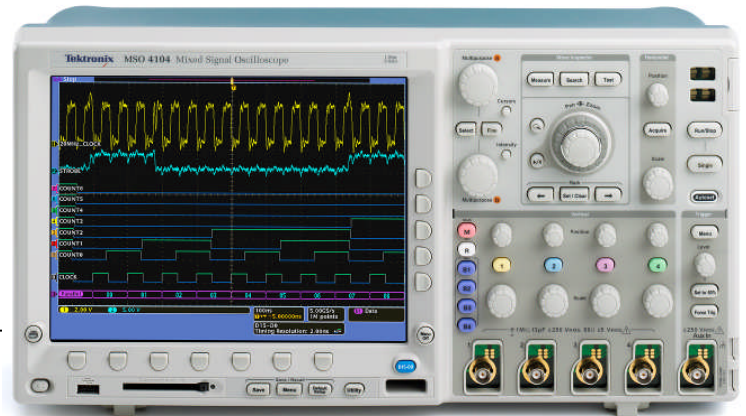
Target Connection

The photo (on right) shows the Tektronix TLA 7000 Logic Analyzer probes connected in to a Xilinx Spartan3E board with its two connections to the target – the acquisition probe plugged into the connectorless board header, and a USB cable plugged into the USB port of the TLA. (For the Spartan3E Starter Kit, the Platform Cable USB is integrated onto the board).



MSO4000 series Mixed-Signal Oscilloscope

The FPGAView software now also supports the 4000 series MSOs. See the photo on right for an example. FPGAView software can control the MSO over an Ethernet or USB link. When the user switches the LA Core input bank, the signal names assigned to the selected bank are written to the scope and display on the left side of the waveform.



Features Summary

FPGAView

- Supports Virtex, Virtex2, Virtex4, Virtex5, Spartan2, Spartan3 and Spartan3E Xilinx devices
- Supports JTAG USER1 or 2 channels, plus channels 3 and 4 for Virtex4 and 5 devices
- Works with multiple devices on the same JTAG chain
- Automatically updates TLA or MSO channel names when selecting a different signal bank
- Supports multiple FPGA devices through JTAG chaining
- PC Windows user interface
- Same software used on TLA integrated Windows or separate host PC
- Updates channel names for the MSO4000 series from a host PC when connected over USB or Ethernet
- User can define a TLA setup file for each bank, making it easy and automatic to reconfigure channel groupings

LA Core

- State (synchronous) or Timing (asynchronous) acquisition modes
- 1, 2, 4, 8, 16, 32, or 64 signal banks
- 4 to 128 signals per bank
- Rising or falling clock edge selection
- Registered or unregistered inputs to assist in meeting timing closure
- Includes General Purpose Inputs and Outputs (GP I/O); selectable in groups of 8 bits up to 64 bits
- GP Inputs useful to scan out static state information
- GP Outputs useful to set modes, toggle wires, control debug
- Can be registered or unregistered; rising or falling clock edge
- Signal bank selection and GP Inputs/Outputs controlled from Xilinx Platform Cable USB
- Some Xilinx development boards such as Spartan3E Starter Kit have embedded the USB cable onto the board
- Requires no BUFPGs or Block RAM resources

OCIGen

- User selects all LA Core options via GUI
- Scans HDL code (Verilog or VHDL) for signals
- Connects up the user's signals to the LA Core for tracing
- Generates connection to the Xilinx JTAG port (USER1-4)
- Installs the LA Core into the user's HDL code.
- Signal names remain intact throughout the design flow and are not removed or modified by other operations in the flow

Hardware Requirements

- Tektronix Logic Analyzer Series supported are: TLA600, TLA5000, TLA700, TLA7000
- Tektronix MSO4000 series and Windows PC
- Target board with at least one Xilinx FPGA, JTAG connection, and at least one TLA or MSO probe connection

Software Requirements

- Xilinx ISE8.2i or later
- ChipScope Pro 9.1i if Xilinx ISE 9.1i is used
- Xilinx ISE9.2i or later (ChipScope Pro not required)
- Xilinx Platform USB Cable for programming
- Tektronix TLA software version 4.3, 5.0 or 5.1, or MSO4000 series mixed-signal oscilloscope

Product Codes

FPGAVIEW-X-TLA	FPGAVIEW, Xilinx FPGA, TLA or PC NIC host license
FPGAVIEW-X-TLA-F	FPGAVIEW, Xilinx FPGA, TLA, floating network server license
FPGAVIEW-X-MSO	FPGAVIEW, Xilinx FPGA, MSO serial number license
FPGAVIEW-X-MSO-PC	FPGAVIEW, Xilinx FPGA, MSO, PC NIC license



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