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Digital Signal Processing on the Industry-Standard MIPS® Architecture

*Radhika Thekkath
Fall Processor Forum, 2004*

Introducing the MIPS® DSP ASE

- **DSP extension** to the MIPS32® and MIPS64® architectures in the integer pipeline
 - Integrates functionality
- New instructions and new architectural state
 - Performance improvement for many applications
 - 5-10% additional core area
- Full development support

***Enhancing the MIPS® Architecture with a
DSP Extension for Lower System Costs***

Agenda

- MIPS® Markets
 - DSP Application Example
- Market Drivers for Signal Processing
- DSP ASE Details
 - Performance Benefits
 - Tools and Infrastructure Support
- Summary

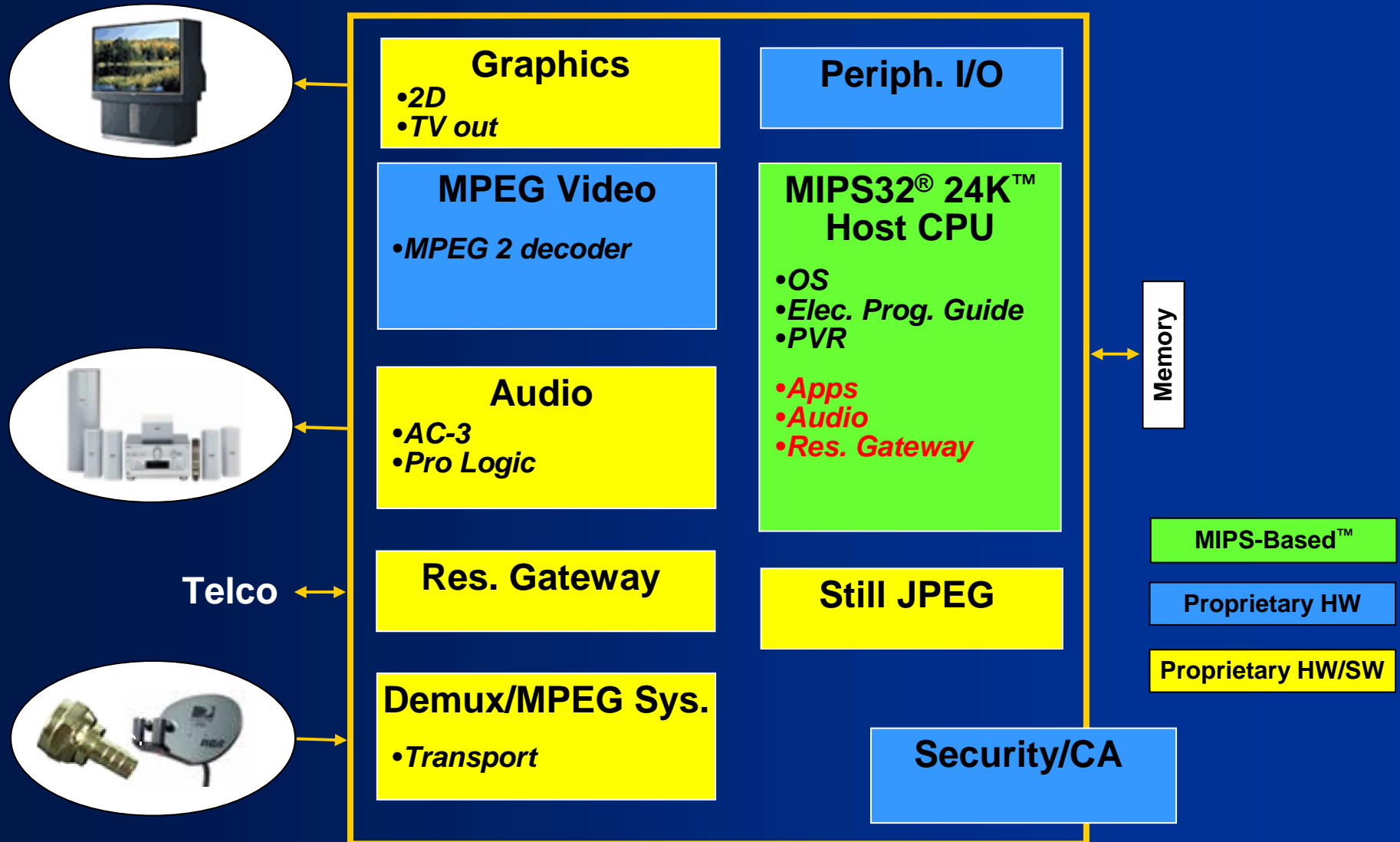
MIPS® Market Leadership

- Internet Backbone **40%**
- DVD Recorders **75%**
- IDTVs **40%**
- DSL Modems **40%**
- Digital STBs **40%**
 - Cable STBs **76%**
- Office Automation **48%**

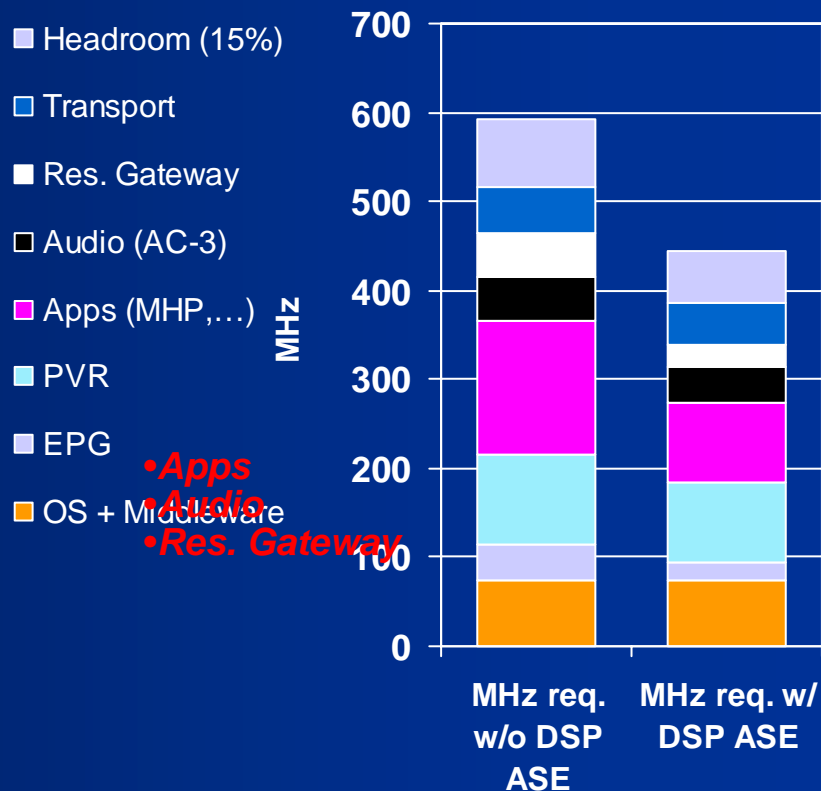
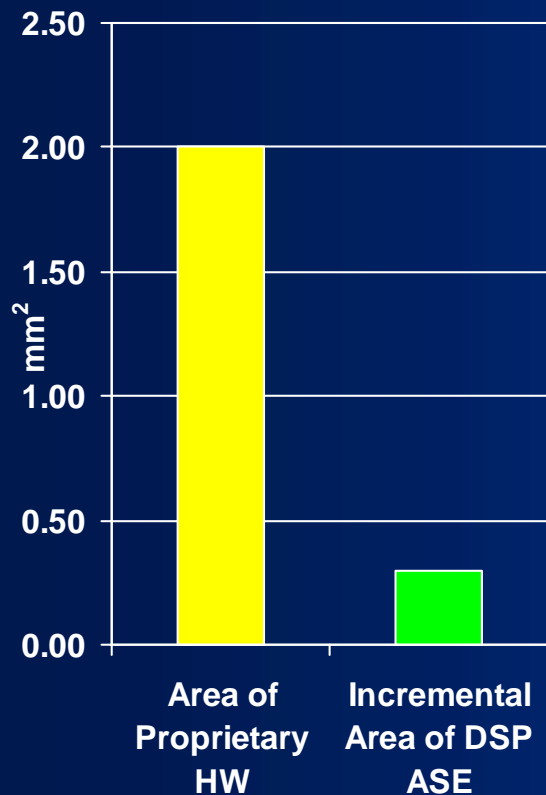


*Sources: IDC, Semico, In-Stat, Iconocast and MIPS Technologies.
Values are percentage of W.W. box shipments.*

Advanced Set-Top Box SOC



STB SOC Benefits with MIPS® DSP ASE



DSP Algorithms Need Less MHz and Area

Market Drivers For Signal Processing

Consumer Market Drivers

- Lower system costs
 - Integrated DSP functions in the host yield smaller SOCs and **cost-effective systems**
 - Single tool chain for signal processing and host
 - MIPS ecosystem
- Feature creep and evolving standards
 - **Programmability** allows easy adaptation to changing standards
 - Synthesizable **performance** leader
 - Increase product lifespan

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Applicability of the MIPS® DSP ASE



Algorithm

DSP ASE feature

Still JPEG
Printer Imaging

8-Bit Data



Voice Codecs, etc
MP3, MPEG-2 Audio ...
V.90 ...
Other General DSP

16-Bit Data



AC-3, MPEG-2 AAC ...
Communication

32-Bit Data

MIPS® DSP ASE Details

What is the MIPS® DSP ASE?

Typical DSP-Like Instructions

- SIMD (8/16/32)
- Saturating fractional math
- MAC/dot-product
- Expand/reduce
- Absolute
- Bit-reverse
- Etc

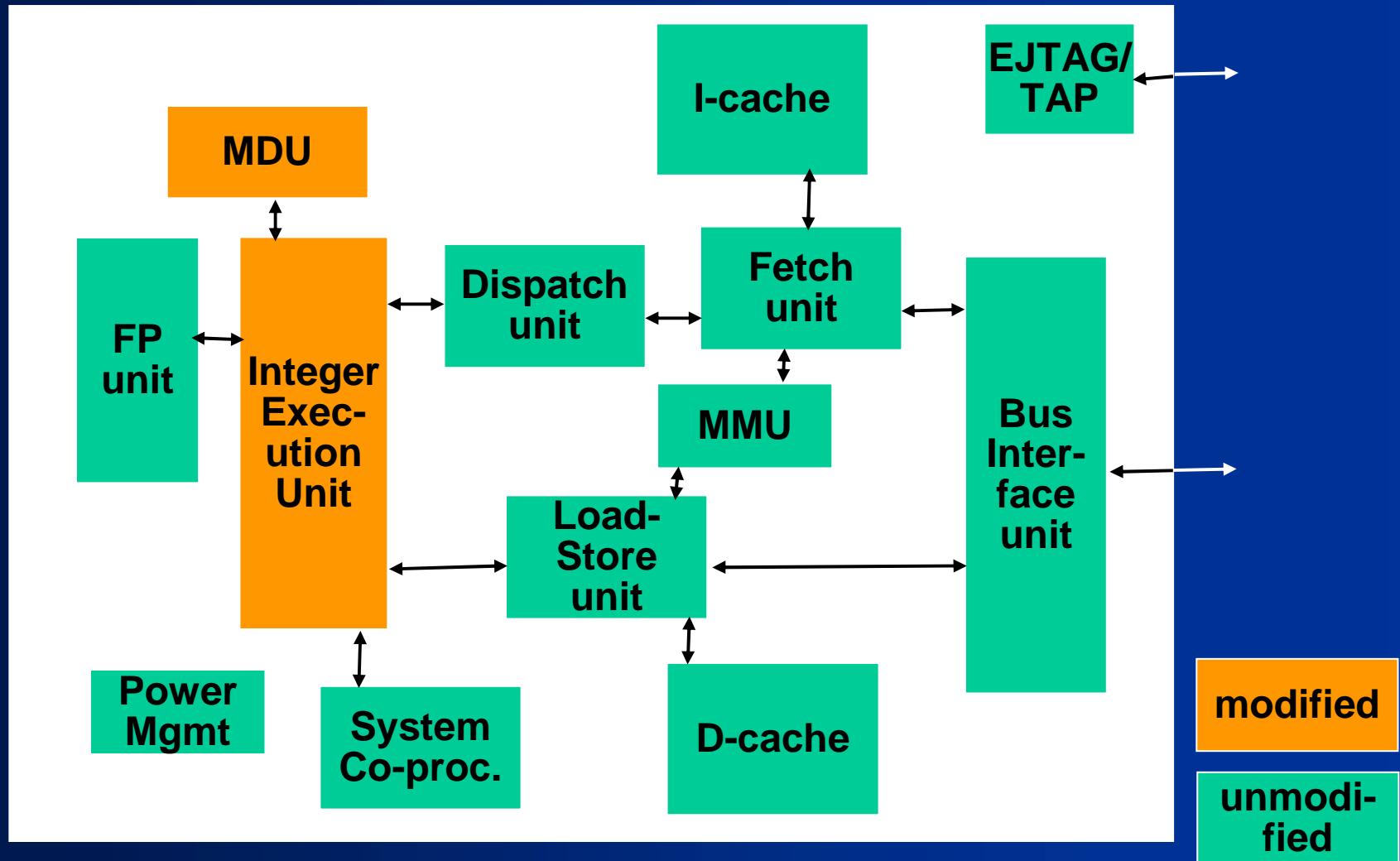
Key Features

- Complex multiply support
- Variable bit insert
- Variable bit extract
- Virtual circular buffers
- Etc

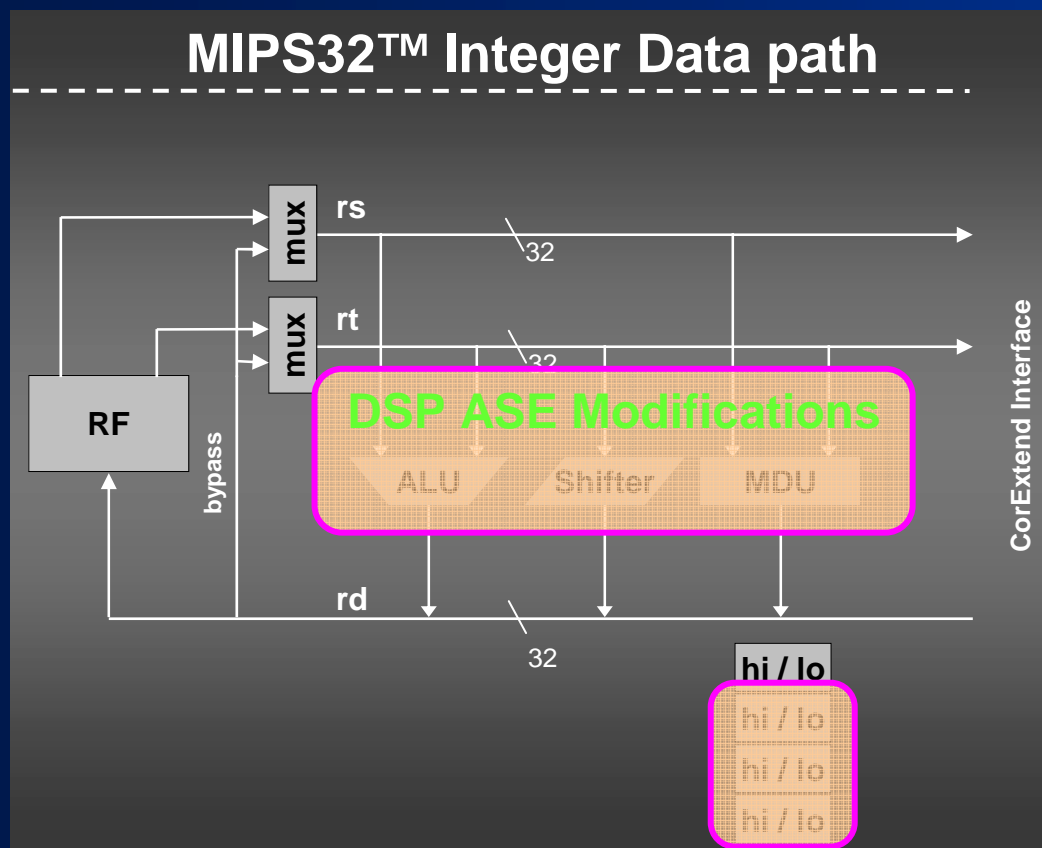
New State

- Accumulators
- DSP Control

Core Blocks Modified for the DSP ASE



DSP ASE Block Diagram (simplified)



- Modifications to existing structures
- Reuse integer data-path
- **5-10% core area increase!**

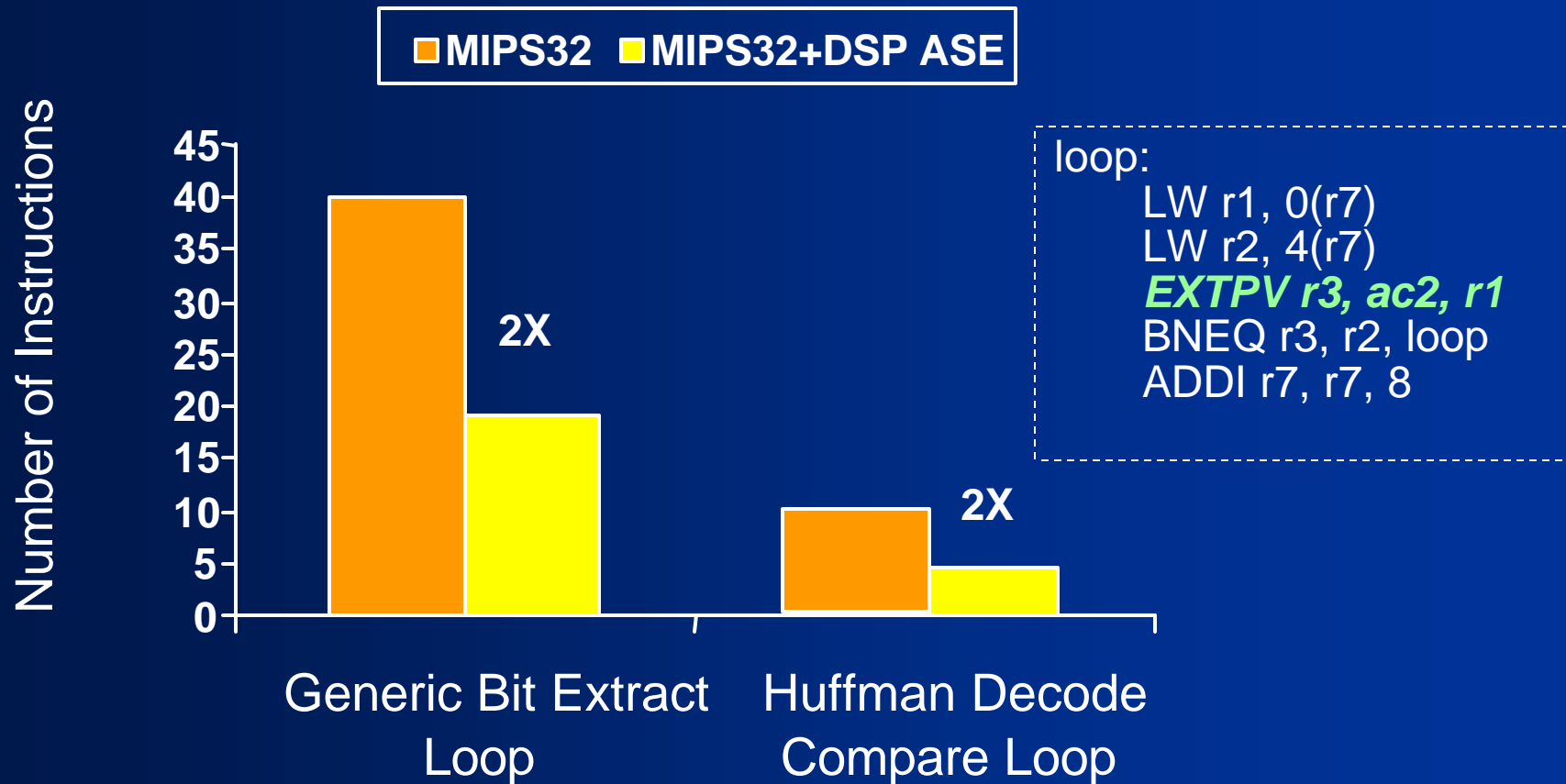
MIPS® DSP ASE Key Feature Example

Example – Efficient Bit Extraction

- Many embedded applications use streaming input data
 - Video, audio, communication packets, etc.
- The issue with formatted streaming data
 - **Variability** in the field widths of packet headers
 - Extract operation needs a different **shift and mask value** per width – inherently inefficient

MIPS® DSP ASE Makes the Variable Bit Extraction Process Very Efficient

24KE Performance Benefit - Variable Bit Extraction



Bit Extract breaks down streams of data

Huffman Compression used in Multimedia and Communications

Variable Bit Extract using the DSP ASE



LW r10, 0(r9)

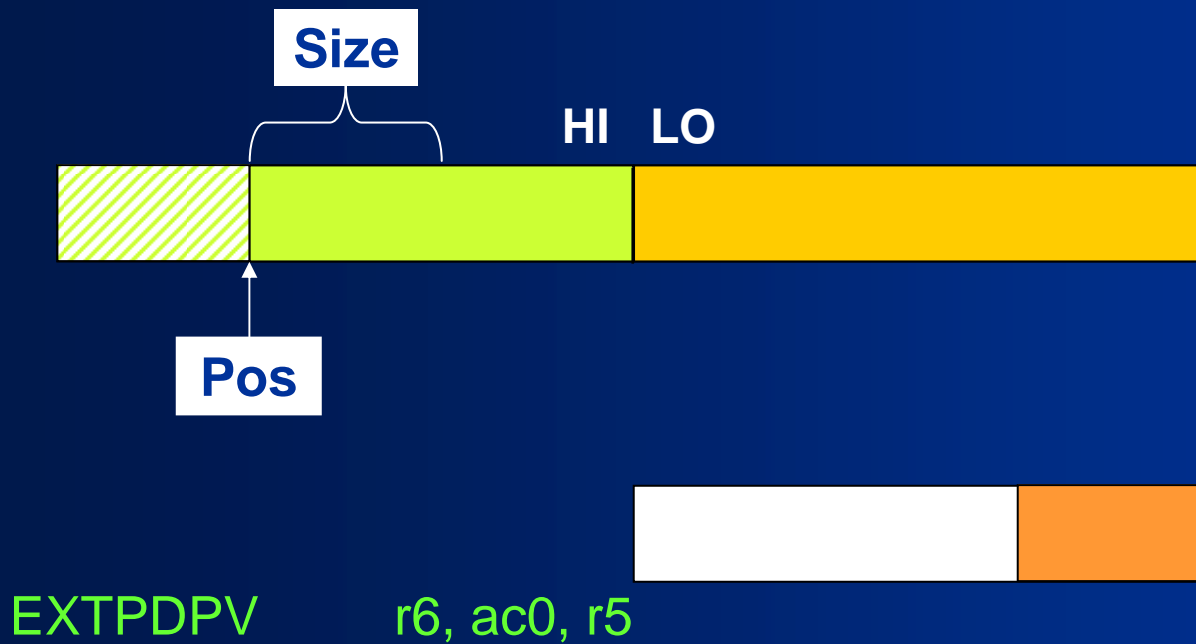
LW r11, 4(r9)

MTHI r10,ac0

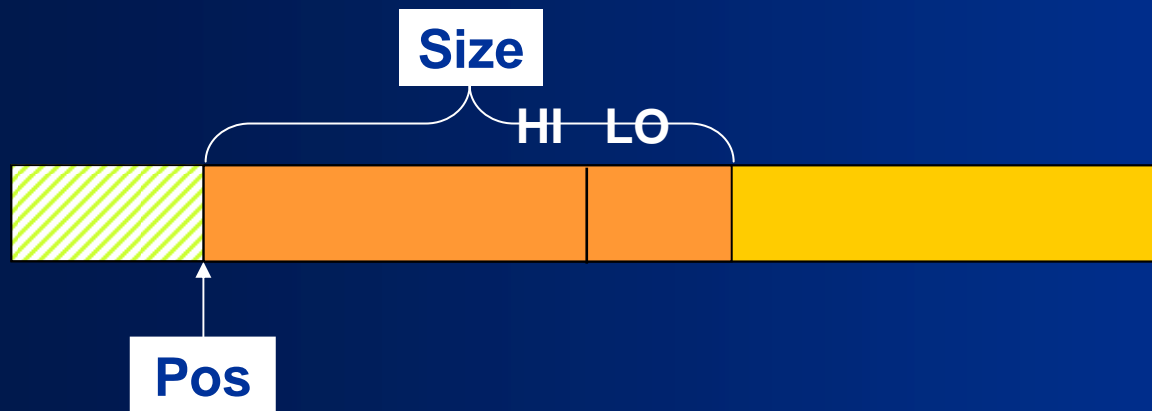
MTLO r11,ac0

LI r5, size

Variable Bit Extract using the DSP ASE



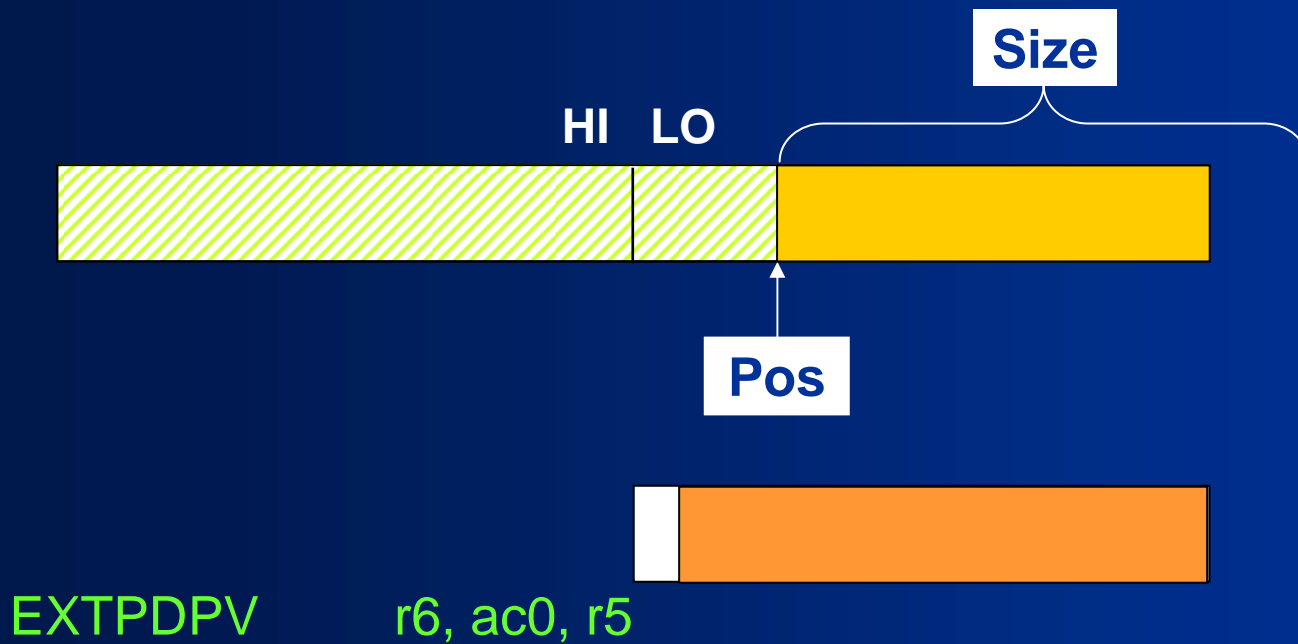
Variable Bit Extract using the DSP ASE



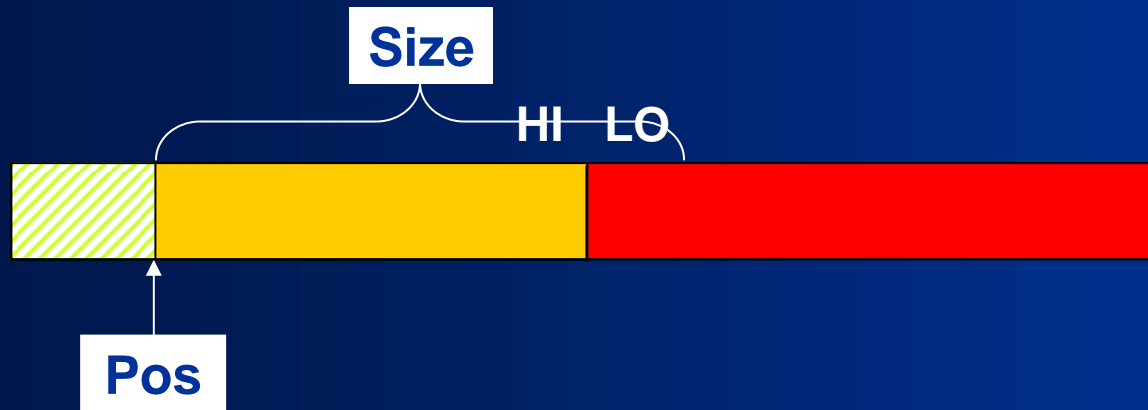
Recalculate size

LI r5, size

Variable Bit Extract using the DSP ASE



Variable Bit Extract using the DSP ASE

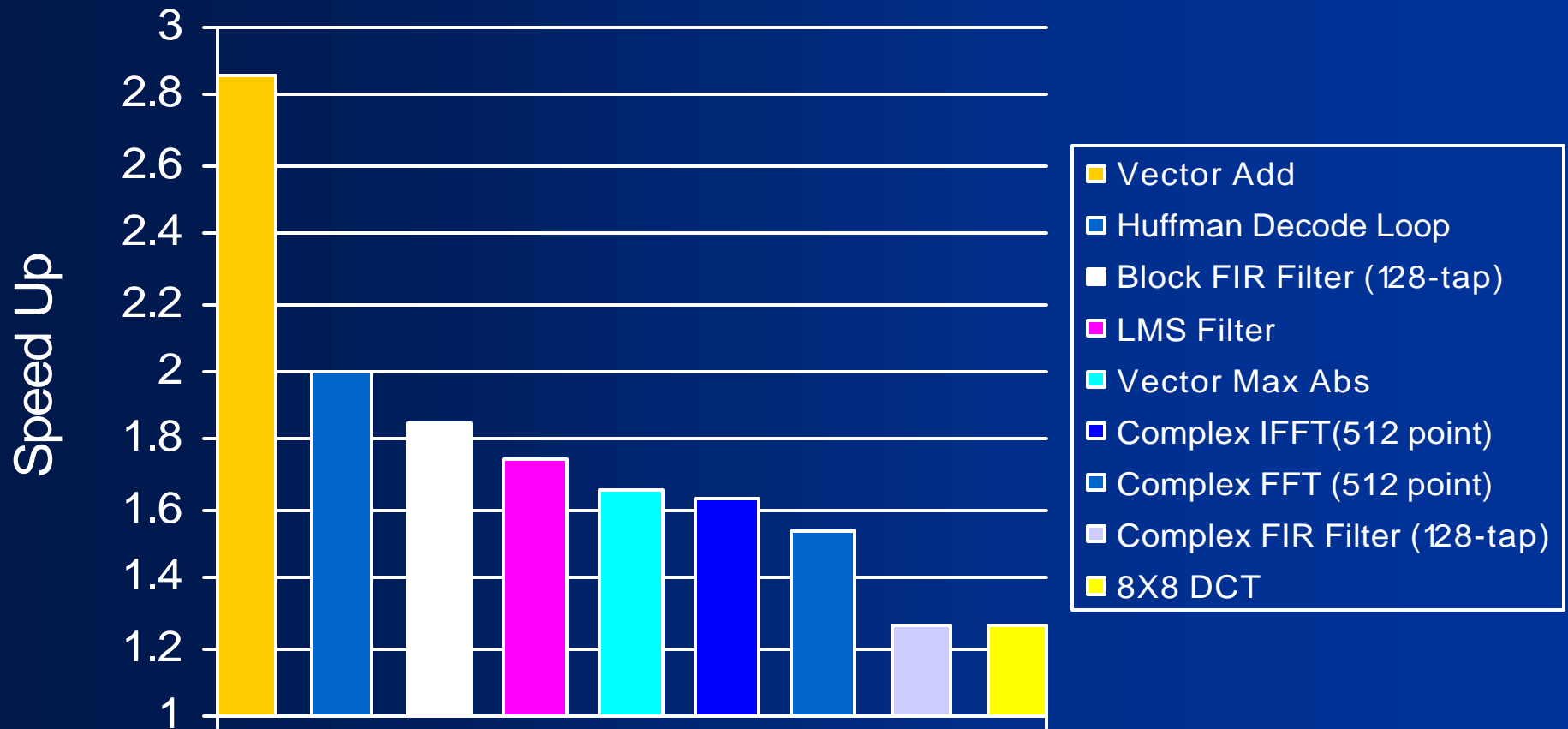


Respond to underflow

LW r10, 8(9)

MTHLIP ac0, rs

DSP Algorithm Speedup



**Speedup Compared to Hand-Optimized MIPS32
Assembly Implementation on a 24K Core**

MIPS® DSP ASE Software Support

Application Layer

- Audio, VoIP, etc.

MIPS Linux

- Support new context

MIPS DSP Library

- Common DSP routines tuned for DSP ASE
- Filters, FFT, DCT, Correlation, etc.

MIPS Toolkit

- Compiler, Assembler, Debuggers, etc
- Simulator
- Performance analysis tools

MIPS DSP ASE

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